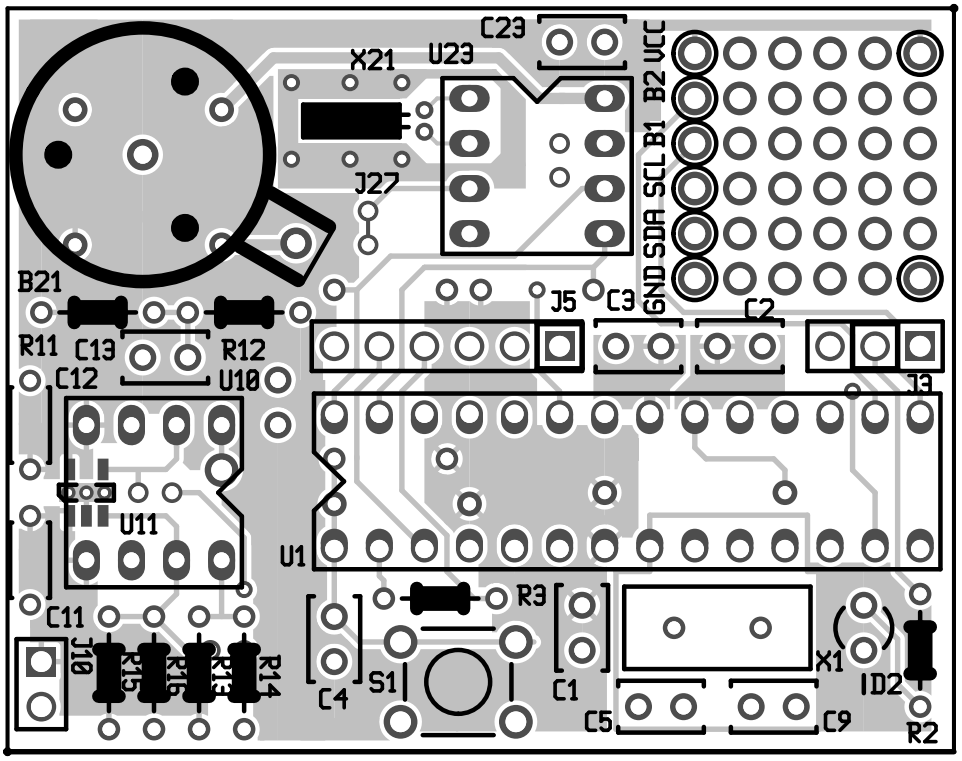


PICO1TRCL Description

The PICO1TRCL is a low-cost microcontroller development board that is compatible with the Arduino development tools. The board is 2.1” x 1.65” and all the I/O pins from the ATmega328 are brought out on 2 rows of 14 pins (300mil spacing).

Features

- **2.1” x 1.65”**
- Replaceable and upgradeable CPU
- Compatible with the Arduino development tools.
- ATmega328P running at 12MHz
- Dual output voltage LDO – 3.3V/2.2V
- Low LDO I_Q – 900nA (SMD), 15μA (TH)
- 0.6” x 0.6” prototyping area
- Real-time clock with two alarms (I2C interface)
- Two rows of 14 pins (300mil spacing) with all ATmega328 I/O functions.
- Six pin header for FTDI TTL-232R-3V3 cable.
- Debug LED that can be jumpered to Pin 7 or disconnected.
- A/D reference supply filtered per Atmel specification.
- Reset circuit per Atmel specification.

1 Assembling the PICO1TRCL

Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

Do not cut any of the U1 socket pins until you have determined which pins are needed in your application. All of the PICO1TRCL I/O pins are the U1 socket pins. See subsection 1.7 for pin removal information.

The Bill of Materials (BOM) and Component List are in section 6. For full page assembly drawings see Figure 1 (top) and Figure 2 (bottom).

There are two different BOMs and Component Lists – one for the TH kit and one for the SMD kit. The PCB and assembly drawings are common to both kits.

1.1 Bottom Side Components

- D1

  Line the cathode marking on D1 with the cathode marking on the silkscreen

- D21, D22

  Line the cathode marking of D21,D22 with the cathode marking on the silkscreen

- L1

  The value of inductor L1 is not critical. Kits will contain an inductor with a value between 10µH and 20µH

- R1, R22, R23

  10KΩ *(brown, black, black, red, brown)*

- C6

1.2 Real-time Clock Circuit Assembly

- X21 crystal
- U23 socket
- B21 battery holder
- C23

1.3 Power Supply Circuit Assembly

There are two versions of the PICO1TRCL kit – SMD and TH. The SMD kit features a very low I_Q linear regulator in an SMD package (SOT23-5). The TH kits uses a linear regulator in a DIP8-300 package. Both kits use the same PCB.

For the TH kit follow the instructions in subsubsection 1.3.1. For the SMD kit follow the instructions in subsubsection 1.3.2.

Since most applications will never disable the LDO it is recommended that `R15` *be replaced with a jumper wire,* `R16` *be left open and jumper* `J12` *be cut to free up the ATmega328P line connected to* `STBY` *(*`EN` *on the* `SMDLDO`*). These changes should be performed prior to adding the LDO components.*

1.3.1 TH LDO Assembly

Solder the top side components:

- C11, C12, C13
- R11

  845KΩ *(gray, yellow, green, orange)*

- R12

  1MΩ *(brown, black, black, yellow)*

- U10 socket

  MAX822CPA

- J10
- R13, R14 (optional)

  R13 and R14 are used to set the trip-point of the low-battery indicator. These components are not included in the kit. See subsection 3.4 for more information.

1.3.2 SMD LDO Assembly

Solder the top side components:

- U11

  TPS780330220DDC

- C11, C12
- J10

1.4 Microcontroller Circuit Assembly

Solder the top side components:

- C1, C2, C3, C13, C4 (optional).

  C4 is optional and is not included in the kit. It is meant for applications that require additional filtering of the reset line. The reset function that uses the /RTS line from the USB interface will not function with C4 installed.

- D2

  The negative lead of the LED is the short lead. Align the short lead with the negative marking on the PCB.

- R2

  *For 3.3V operation use the 374Ω (orange, violet, yellow, black, brown). For 5V operation use the 1*KΩ *(brown, black, black brown, brown)*

- R3
  10KΩ (brown, black, black, red, brown)
- J3
- J5
- X1, C5, C9
- U1 (socket)

1.5 Electro-mechanical Components

Since the reset switch (S1) is sensitive to washing it should be placed on last. Lightly clean the board after the switch is installed. If water does get into the switch let it dry out before applying power.
Solder the top side components:

- S1

1.6 IC Installation and Test

1.6.1 U23 (DS1337)

Remove the DS1337 from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

1.6.2 U1 (ATmega328P)

Remove the ATmega328P from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

1.6.3 B21 (CR1220 coin cell)

Install a CR1220 coin cell into the battery holder (`B21`) observing the polarity indicated on the holder.

The PICO1TRCL should now be fully functional and is ready to program (see section 5). Depending on the application some of the pins on the U1 socket should be removed (see subsection 1.7).

1.7 Pin Removal

After operation of the PICO1TRCL is verified it is recommended that some of the U1 pins be cut flush to the PCB level. Each application is different and needs to reviewed. Pins like `XTAL1` and `XTAL2` can be affected by stray capacitance and noise. For most applications cutting the `XTAL1`, `XTAL2`, `AREF` and `AVCC` is recommended.

If your application may change over time then leave all pins intact and use care in your layout.

1.7.1 XTAL Pins

The XTAL circuit is susceptible to stray capacitance and noise so pins 9 and 10 should be cut flush to the PCB.

1.7.2 AREF

If you are not using an external analog reference then cut pin 21 flush to the board.

1.7.3 AVCC

If you are not powering the ADC from a different source then pin 20 should be cut flush to the board.

2 IO Connectors

J5 USB header for an FTDI TTL-232R-3V3 cable.

J10 Input power header. See subsection 3.1

3 Electrical Hints

3.1 Power Supply

The PICO1TRCL is powered by a DC input source connected to `J10`. It is recommended that the PICO1TRCL be operated from a 5V supply. The SMD LDO (TPS780330220DDC) kit can be operated up to 5.5V. The TH LDO (MAX882CPA) can be operated up to 11.5V but care needs to be taken so that the maximum junction temperature (T_{jmax}) of the LDO is not exceeded.

3.1.1 Calculating LDO Junction Temperature

The power dissipation in the LDO (SMD or TH) is

$$P_{diss} = V_{drop} \cdot I_{out}$$

where

$$V_{drop} = V_{in} - V_{out}$$

and

V_{in} is the input voltage to the PICO1TRCL

V_{out} is the output voltage of the LDO

I_{out} is the current out of the LDO

The junction temperature of the LDO is

$$T_J = P_{DISS} \cdot R_{\theta JA} + T_{AMBIENT}$$

where

$R_{\theta JA}$ is the thermal resistance of the LDO. The SMD LDO (TPS780330220DDC) has 200°C/W for the SMD LDO (TPS780330220DDC) and 110°C/W for the TH LDO (MAX882CPA).

$T_{AMBIENT}$ is the ambient temperature that the PICO1TRCL is operating at.

For the SMD kit the maximum junction temperature (T_{JMAX}) of the LDO is 125°C, for the TH kit the T_{JMAX} is 150°C.

	I_{OUT}	T_j vs V_{in}		T_{jmax}
		5V	5.5V	
SMD-KIT	150mA	76°C	91°C	125°C
TH-KIT	200mA	63°C	74°C	150°C

Table 1: T_{JMAX} for the PICO1TRCL LDO

3.2 Changing V_{cc} using Software

The LDO on the PICO1TRCL can be changed digitally by the ATmega328P. When the LDO `SET` pin is set to a logic zero the LDO output is set to 3.3V. When the `SET` pin is at logic one the output goes to 2.2V. This is useful for reducing power consumption when the ATmega328P is in sleep mode.

3.3 Enable/Standby Pins

The TH LDO (MAX882CPA) and SMD LDO (TPS780330220DDC) have enable pins. On the TH LDO (MAX882CPA) the enable pin is labeled `STBY`. On the SMD LDO (TPS780330220DDC) it is `EN`. The net on the schematic is labeled `STBY`. A low value disables the LDO, a high value enables it.

Since most applications will never disable the LDO it is recommended that `R15` *be replaced with a jumper wire,* `R16` *be left open and jumper* `J12` *be cut to free up the ATmega328P line connected to* `STBY` *(*`EN` *on the* `SMDLDO`*). These changes will be made to the next revision of the board.*

3.4 Low-Battery Indicator (TH-KIT ONLY)

The TH LDO (MAX882CPA) has a low-battery output (`LBO`) which is an open-drain output that goes low when the `LBI` pin is less the 1.2V. The `R13`, `R14` divider sets the low-battery trip point. The LBI trip point level is –

$$V_{LBITRIP} = 1.2\text{V} \cdot \frac{R_{13} + R_{14}}{R_{14}}$$

If the low-battery indicator is not required short `R13` with a jumper wire and leave `R14` open.

The `LBO` is connected to testpoint 11 (`TP11`). Wire `TP11` to any unused ATmega328P I/O line. Since the `LBO` is an open-drain line it is necessary to use the ATmega328P internal pull-up resistors.

4 Real-Time Clock

The PICO1TRCL real-time clock (RTC) consists of a DS1337 that is powered by a CR1220 coin cell or the PICO1TRCL linear regulator (`U10`). The or'ing diodes, `D21` and `D22`, will output the higher voltage to the RTC (`U23`).

Communication to the DS1337 is through the I²C interface (a.k.a. two-wire or TWI). The I²C pullup resistors are on board (10KΩ). The interrupt lines, `/INTA` and `/INTB` are jumpered to `PC3` (Arduino pin 17) and `PC0` (Arduino pin 14) respectively. There are no pullup resistors on the interrupt lines. If external pullups are not added then the internal pullups of the ATmega328P need to be used.

Programming the RTC requires a software library for the DS1337 and for the TWI interface. Both of these libraries are on the wiblocks site.

4.1 I²C Pullup Resistors

The maximum bus capacitance of the I²C bus is 400pF. Unless a large number of devices are on the bus or devices are connected using long cables PICO1TRCL system will not get close to this limit. The DS1337 represents a maximum load of 10pF.

The minimum pullup resistance is 966Ω ($\frac{V_{CC}-0.4\text{V}}{3\text{mA}}$). The maximum value pullup resistance is

$$R_{pullup(max)} = \begin{cases} \frac{1000\text{nS}}{C_{BUS}} & \text{if } F_{SCL} \leq 100\text{kHz}, \\ \frac{300\text{nS}}{C_{BUS}} & \text{if } 100\text{kHz} < F_{SCL} \leq 400\text{kHz}. \end{cases}$$

where C_{BUS} is the maximum bus capacitance, , and V_{CC} is 3.3V for the PICO1TRCL.

With a 100pF load (10 times the DS1337 load), the maximum resistance for 400kHz operation is 3KΩ. For 100kHz the maximum resistance is 10KΩ. If only the DS1337 is on the I²C bus the maximum resistances would be 100KΩ (100kHz) and 30KΩ (400kHz). The minimum resistance, which is not dependent on bus capacitance, is 966Ω for any operating frequency and C_{BUS}. (Atmel, 2009a)

CBUS	**100**pF		**400**pF	
Frequency	**Resistance**		**Resistance**	
	Min	**Max**	**Min**	**Max**
100kHz	1150Ω	10KΩ	1150Ω	2500Ω
400kHz	1150Ω	3KΩ	–Not Practical–	

Table 2: I²C Pullup Resistors

4.2 DS1337 Interrupt Lines

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PC3 (Arduino pin 17) and PC0 (Arduino pin 14) respectively. To disconnect `/INTA` cut jumper `J24`. To disconnect `/INTB` cut jumper `J27`.

There are no pullup resistors connected to the interrupt lines. To use the interrupt lines with the ATmega328P the internal pull-up resistors need to be enabled. For the ATmega328P 20KΩ $\leq R_{pullup} \leq$ 50KΩ which is sufficient to pullup the DS1337 lines. (Atmel, 2009b).

4.3 RTC Battery Life

The DS1337 operates with a V_{CC} from 1.8V to 5.5V. When power is removed from the PICO1TRCL the DS1337 is in standby mode and the maximum standby current is 1.5μA(Maxim, 2009a). The CR1220 coin cell has a capacity of 40mAH (to 2V). The battery life is $\approx$ 26000 hours.

4.4 Prototype Area

To the right of the RTC there is a small prototype area. Eight test points are provided to connect circuitry from the prototype area to the ATmega328P. With the PICO1TRCL rotated 90 degrees clockwise there is a row of six pins at the top and two pins at the bottom. The pinout is shown in Table 3.

Pin Name	Arduino Number	Notes
GND		left top
SDA (PC4)	A4	
SCL (PC5)	A5	
PB1	9	
PB2	10	
VCC		right top
GND		left bottom
VCC		right bottom

Table 3: Prototype Area Pins

4.5 Debug LED

The debug LED, D2, can be connected to U1 pin 13 (PD7) of the ATmega328P or left disconnected. U1 pin 13 corresponds to Arduino pin 7

LED jumper in the disconnected position

LED jumper in the PD7 position

4.6 Pinout

The input and output pins for the PICO1TRCL are the socket pins of the microcontroller (U1). The pinout is listed in Table 4.

Pin Number	Pin Name	Arduino Number	Notes
2	RXD	0	
3	TXD	1	
4	PD2	2	
5	PD3	3	
6	PD4	4	
11	PD5	5	
12	PD6	6	
13	PD7	7	Debug LED
14	PB0	8	
15	PB1	9	
16	PB2	10	
17	PB3	11	MOSI
18	PB4	12	MISO
19	PB5	13	SCK
23	PC0	A0	
24	PC1	A1	
25	PC2	A2	
26	PC3	A3	
27	PC4	A4	SDA
28	PC5	A5	SCL
1	Reset		
9	XTAL1		PB6
10	XTAL2		PB7
7	VCC		
20	AVCC		
21	AREF		
8	GND		
22	GND		

Table 4: U1 Pinout

5 Programming the PICO1TRCL

The PICO1TRCL can be programmed using the Arduino tools (version `0012` or later). Connect an FTDI TTL-232R-3V3 cable to header J5 with the black wire aligned to pin one.

5.1 Selecting the proper board

In order for the Arduino tools to recognize the wiblocks boards additional lines need to be added to the `boards.txt` file. The additional lines are shown in Listing 1 (with annotations). A file containing these adddions can be downloaded from wiblocks. Once `boards.txt` is modified select `wiblocks 328 at 12MHz` from the `Tools->Board` menu.

5.2 Downloading a program

The PICO1TRCL must be rebooted to start the program download. This can be done by pressing the reset button `S1` immediately before starting the download. If your USB port is configured to `set RTS on close` then the reset will occur automatically.

Listing 1: boards.txt Modifications for the PICO1TRCL

```
wiblocks_328.name=wiblocks 328 at 12MHz
wiblocks_328.upload.protocol=stk500
wiblocks_328.upload.maximum_size=30720
wiblocks_328.upload.speed=19200
wiblocks_328.bootloader.low_fuses=0xff
wiblocks_328.bootloader.high_fuses=0xdd
wiblocks_328.bootloader.extended_fuses=0x00
wiblocks_328.bootloader.path=atmega328
wiblocks_328.bootloader.file=wiblocks_328.hex
wiblocks_328.bootloader.unlock_bits=0x3F
wiblocks_328.bootloader.lock_bits=0x0F
wiblocks_328.build.mcu=atmega328p
wiblocks_328.build.f_cpu=12000000L
wiblocks_328.build.core=arduino
```

References

Atmel. (2009a). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. , 323. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)

Atmel. (2009b). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. , 314. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)

Atmel. (2009c). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)

Maxim. (2009a, July). DS1337 I2C Serial Real-Time Clock. , 2-3. (Retrieved September 30, 2009, from http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf)

Maxim. (2009b, July). DS1337 I2C Serial Real-Time Clock. (Retrieved September 30, 2009, from http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf)

6 Assembly Documentation and Schematics

Table 5: Bill of Materials

Kit: PICO1TRCL-SMD-KIT

Qty	Reference	Part Number	Description
1	B21	CON_BAT__Keystone_500	connector, battery, CR1220
5	C1, C2, C3, C6, C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
2	C5, C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
2	C11, C12	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
1	D1	DIOA-1N4148	diode, 1N4148
1	D2	LEDR-1T-GRN-2M00	LED, T1, Green
2	D21, D22	DIOA-BAT41	diode, BAT41
1	J3	HDR_BR-3X1-100M	header, 3x1, 100mils
1	J5	HDR_BR-6X1-100M	header, 6x1, 100mils
1	J10	HDR_BR-2X1-100M	header, 2x1, 100mils
1	L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
4	R1, R3, R22, R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
1	R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
1	S1	SW__Panasonic_EVQ-PAE04M	pushbutton
1	U1	IC__ATMEL_ATmega328-20PU	ATmega328-20PU, 32K/1K/2K, 20MHz
1	U11	TI_TPS780330220DDC	
1	U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1337+
1	X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
1	X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
1		DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
1		JMP__Adamtech_MSBHG	Shunt with handle
1		DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
1		wiblock_PICO1TRCL-PCB	

Table 6: Component List

Kit: PICO1TRCL-SMD-KIT

Reference	Part Number	Description
B21	CON_BAT__Keystone_500	connector, battery, CR1220
C1	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C6	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C5	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C11	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
C12	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
D1	DIOA-1N4148	diode, 1N4148
D2	LEDR-1T-GRN-2M00	LED, T1, Green
D21	DIOA-BAT41	diode, BAT41
D22	DIOA-BAT41	diode, BAT41
J3	HDR_BR-3X1-100M	header, 3x1, 100mils
J5	HDR_BR-6X1-100M	header, 6x1, 100mils
J10	HDR_BR-2X1-100M	header, 2x1, 100mils
L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
R1	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R3	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R22	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
S1	SW__Panasonic_EVQ-PAE04M	pushbutton
U1	IC__ATMEL_ATmega328-20PU	ATmega328-20PU, 32K/1K/2K, 20MHz
U11	TI_TPS780330220DDC	
U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1337+
X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
	DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
	JMP__Adamtech_MSBHG	Shunt with handle
	DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
	wiblock_PICO1TRCL-PCB	

Table 7: Bill of Materials

Kit: PICO1TRCL-TH-KIT

Qty	Reference	Part Number	Description
1	B21	CON_BAT__Keystone_500	connector, battery, CR1220
6	C1, C2, C3, C6, C13, C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
2	C5, C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
2	C11, C12	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
1	D1	DIOA-1N4148	diode, 1N4148
1	D2	LEDR-1T-GRN-2M00	LED, T1, Green
2	D21, D22	DIOA-BAT41	diode, BAT41
1	J3	HDR_BR-3X1-100M	header, 3x1, 100mils
1	J5	HDR_BR-6X1-100M	header, 6x1, 100mils
1	J10	HDR_BR-2X1-100M	header, 2x1, 100mils
1	L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
4	R1, R3, R22, R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
1	R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
1	R11	RES-845K-0W125-1T00	resistor, 845K, 1/8W, 1%
1	R12	RES-1M00-0W125-1T00	resistor, 1.0M, 1/8W, 1%
1	S1	SW__Panasonic_EVQ-PAE04M	pushbutton
1	U1	IC__ATMEL_ATmega328-20PU	ATmega328-20PU, 32K/1K/2K, 20MHz
1	U10	Maxim_MAX882CPA	
1	U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1337+
1	X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
1	X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
2		DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
1		JMP__Adamtech_MSBHG	Shunt with handle
1		DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
1		wiblock_PICO1TRCL-PCB	

Table 8: Component List

Kit: PICO1TRCL-TH-KIT

Reference	Part Number	Description
B21	CON_BAT__Keystone_500	connector, battery, CR1220
C1	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C6	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C13	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C5	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C11	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
C12	CAPR-2U20-10V-X5R-5MM	capacitor, ceramic, 2.2uF, 10%, 10V, X5R
D1	DIOA-1N4148	diode, 1N4148
D2	LEDR-1T-GRN-2M00	LED, T1, Green
D21	DIOA-BAT41	diode, BAT41
D22	DIOA-BAT41	diode, BAT41
J3	HDR_BR-3X1-100M	header, 3x1, 100mils
J5	HDR_BR-6X1-100M	header, 6x1, 100mils
J10	HDR_BR-2X1-100M	header, 2x1, 100mils
L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
R1	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R3	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R22	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
R11	RES-845K-0W125-1T00	resistor, 845K, 1/8W, 1%
R12	RES-1M00-0W125-1T00	resistor, 1.0M, 1/8W, 1%
S1	SW__Panasonic_EVQ-PAE04M	pushbutton
U1	IC__ATMEL_ATmega328-20PU	ATmega328-20PU, 32K/1K/2K, 20MHz
U10	Maxim_MAX882CPA	
U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1337+
X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
	DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
	JMP__Adamtech_MSBHG	Shunt with handle
	DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
	wiblock_PICO1TRCL-PCB	

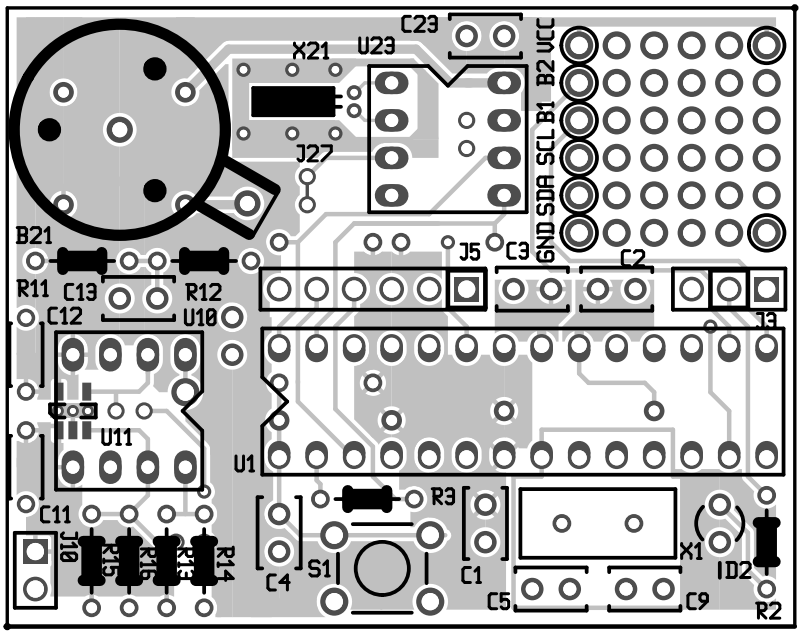


Figure 1: PICO1TRCL Top Side Assembly Drawing (Rev 1)

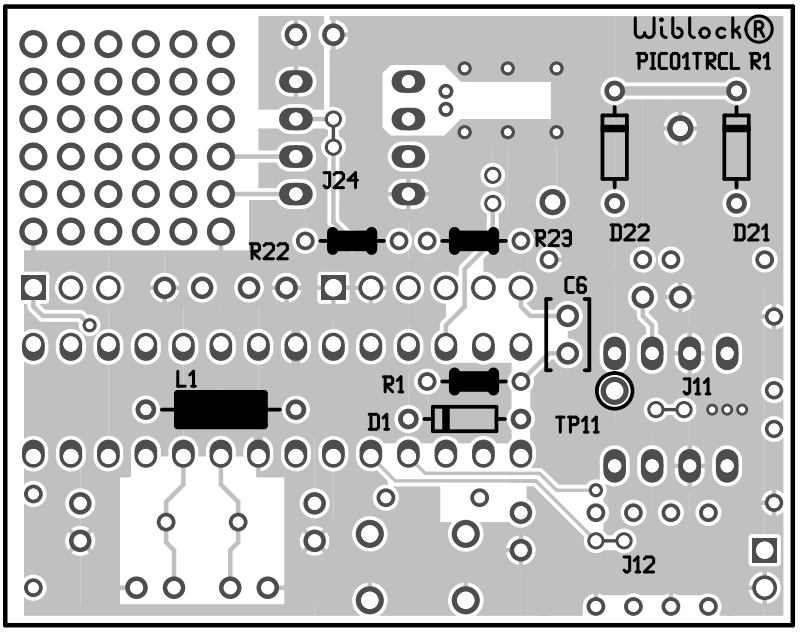


Figure 2: PICO1TRCL Bottom Side Assembly Drawing (Rev 1)

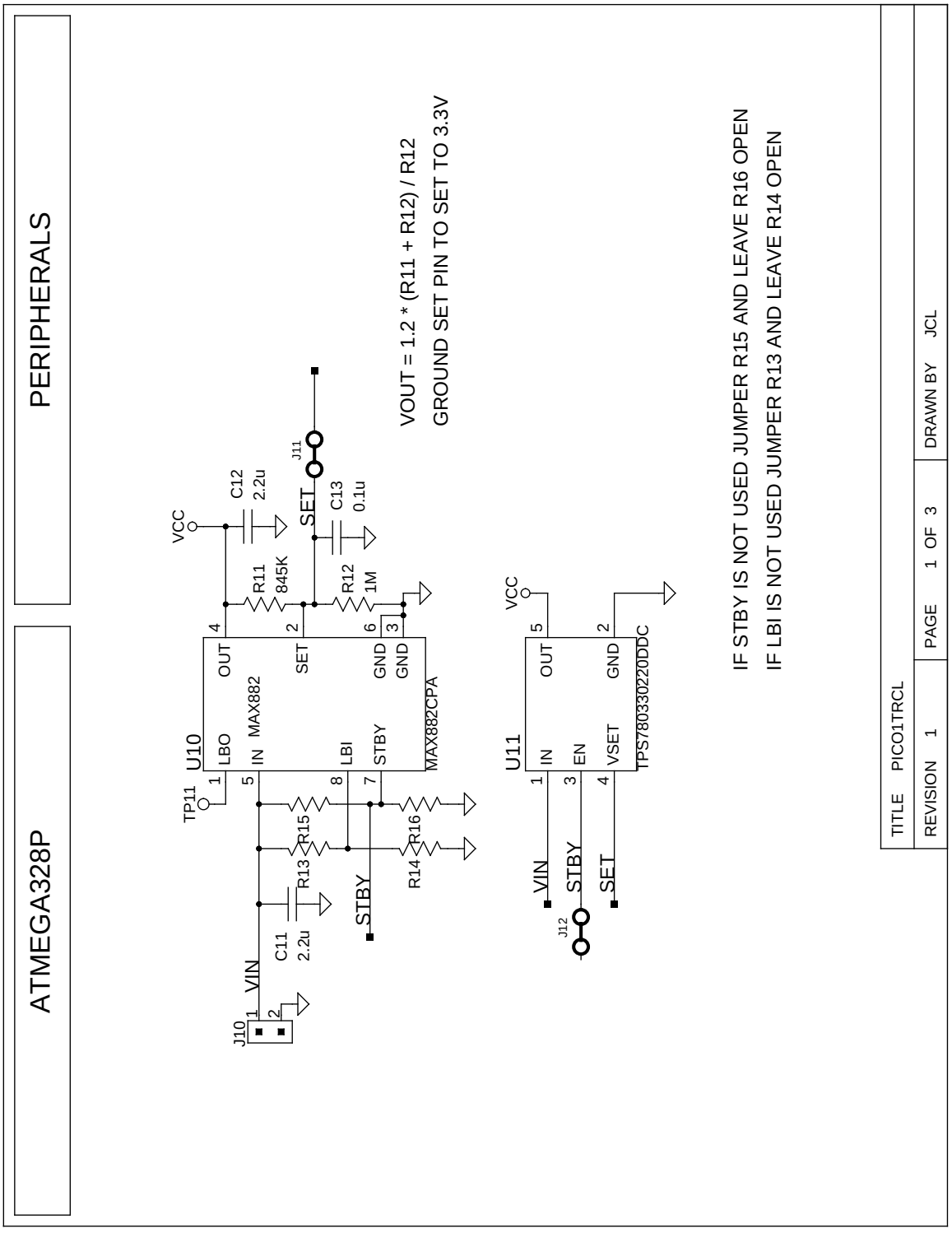


Figure 3: PICO1TRCL (Rev 1)

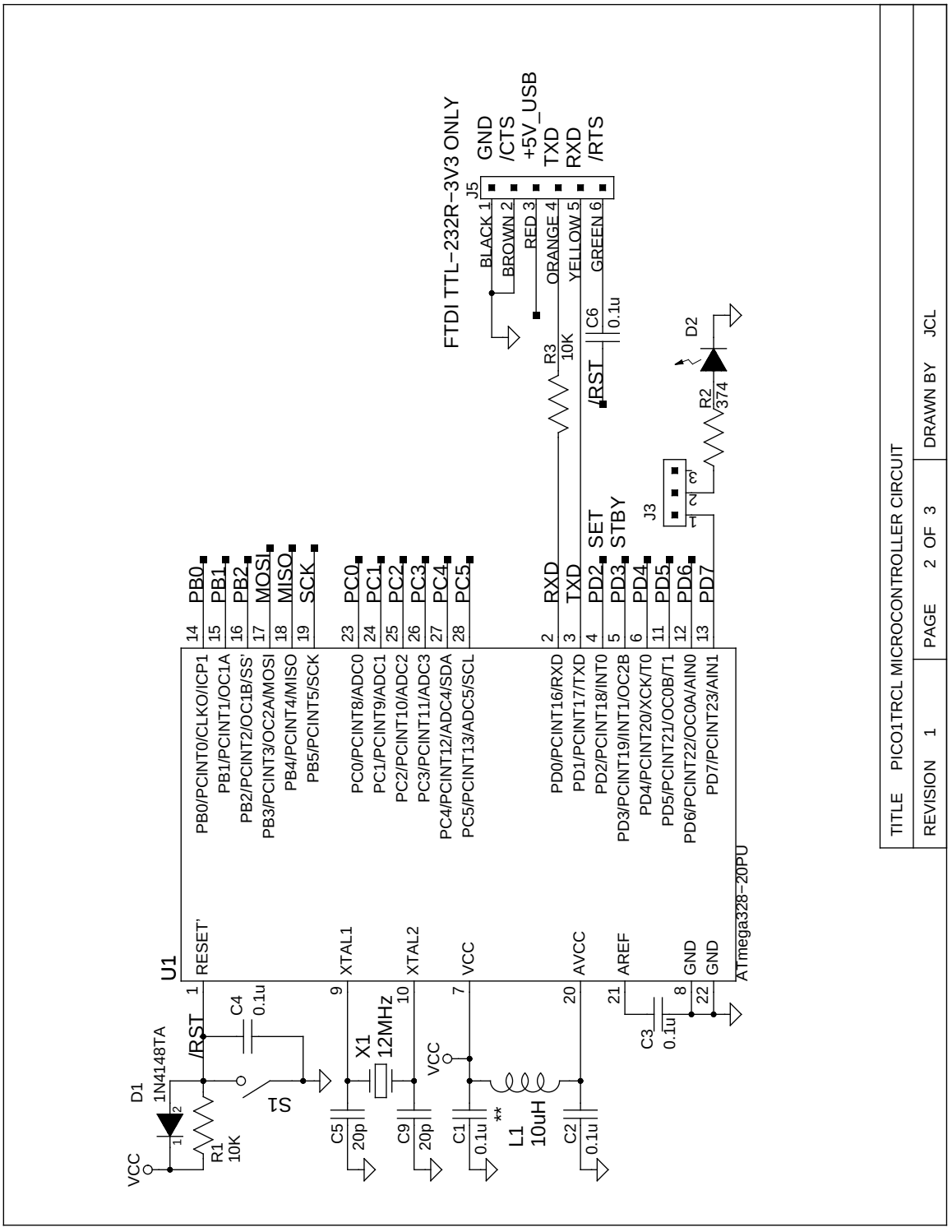


Figure 4: PICO1TRCL (Rev 1)

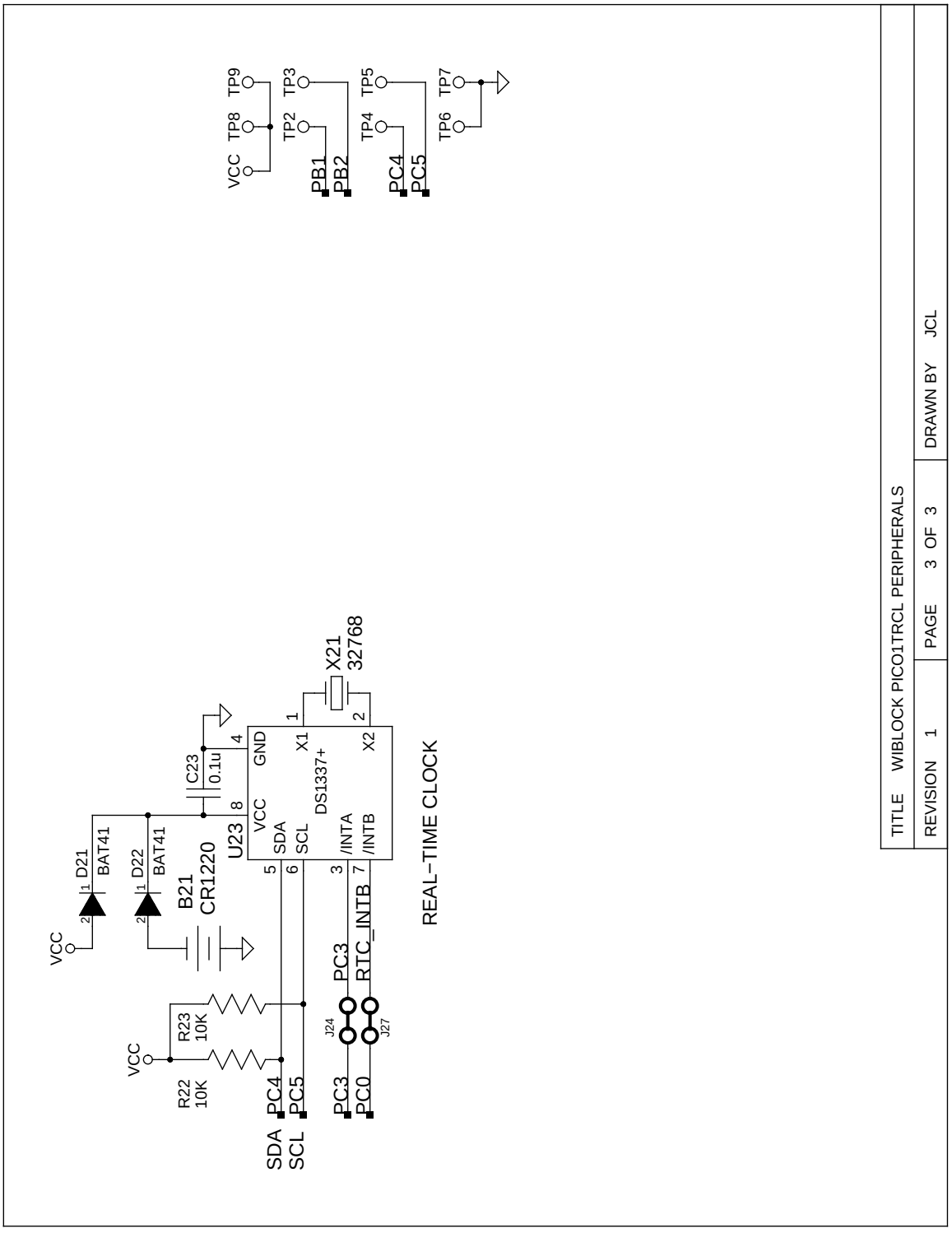


Figure 5: PICO1TRCL (Rev 1)

PRELIMINARY

19-4652; 7/09

DALLAS SEMICONDUCTOR MAXIM

DS1337
I²C Serial Real-Time Clock

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V. I^2C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with V_{CC} as low as 1.3V.

APPLICATIONS

Handhelds (GPS, POS Terminal, MP3 Player)

Consumer Electronics (Set-Top Box, VCR/Digital Recording)

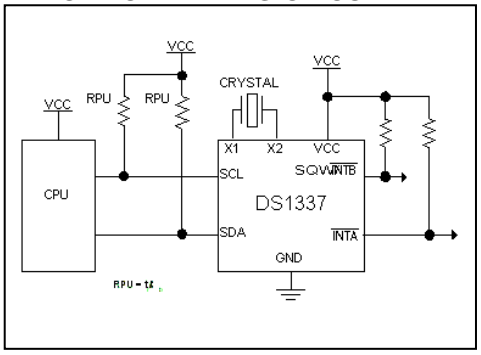
Office Equipment (Fax/Printer, Copier)

Medical (Glucometer, Medicine Dispenser)

Telecommunications (Router, Switch, Server)

Other (Utility Meter, Vending Machine, Thermostat, Modem)

TYPICAL OPERATING CIRCUIT



FEATURES

- **Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100**
- **Available in a Surface-Mount Package with an Integrated Crystal (DS1337C)**
- **I^2C Serial Interface**
- **Two Time-of-Day Alarms**
- **Oscillator Stop Flag**
- **Programmable Square-Wave Output Defaults to 32kHz on Power-Up**
- **Available in 8-Pin DIP, SO, or µSOP**
- **-40°C to +85°C Operating Temperature Range**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1337+	-40°C to +85°C	8 DIP (300 mils)	DS1337
DS1337S+	-40°C to +85°C	8 SO (150 mils)	DS1337
DS1337U+	-40°C to +85°C	8 µSOP	1337
DS1337C#	-40°C to +85°C	16 SO (300 mils)	DS1337C

+ Denotes a lead(Pb)-free/RoHS-compliant device.
 # Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.
† A "+" anywhere on the top mark denotes a lead-free device. A "#" denotes a RoHS-compliant device.

Pin Configurations appear at end of data sheet.

***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.3V to +6.0V
Operating Temperature Range (Noncondensing).....-40°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	Full operation	1.8	3.3	5.5	V
	V_{CCT}	Timekeeping (Note 5)	1.3		1.8	V
Logic 1	V_{IH}	SCL, SDA	0.7 x V_{CC}		V_{CC} + 0.3	V
		$\overline{INTA}$, SQW/$\overline{INTB}$			5.5	
Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS—Full Operation

(**V_{CC} = 1.8V to 5.5V**, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 2)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 3)	-1		+1	µA
Logic 0 Output (V_{OL} = 0.4V)	I_{OL}	(Note 3)			3	mA
Active Supply Current	I_{CCA}	(Note 4)			150	µA
Standby Current	I_{CCS}	(Notes 5, 6)			1.5	µA

DC ELECTRICAL CHARACTERISTICS--Timekeeping

(**V_{CC} = 1.3V to 1.8V,** T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timekeeping Current (Oscillator Enabled)	I_{CCTOSC}	(Notes 5, 7, 8, 9)		425	600	nA
Data-Retention Current (Oscillator Disabled)	I_{CCTDDR}	(Notes 5, 9)			100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 14)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 15)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}			100		ms

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{INTA}$, and SQW/$\overline{INTB}$.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 5: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when $1.8 \le V_{CC} \le 5.5V$. Time and date are maintained when $1.3V \le V_{CC} \le 1.8V$.

Note 10: After this period, the first clock pulse is generated

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \ge$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

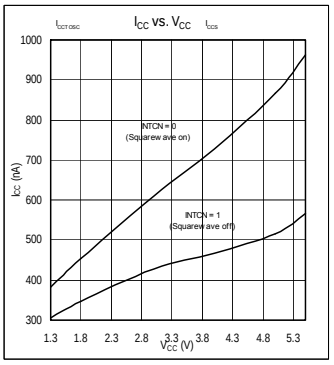
Note 14: C_B—total capacitance of one bus line in pF.

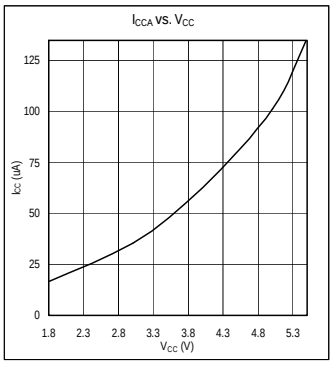
Note 15: Guaranteed by design. Not production tested.

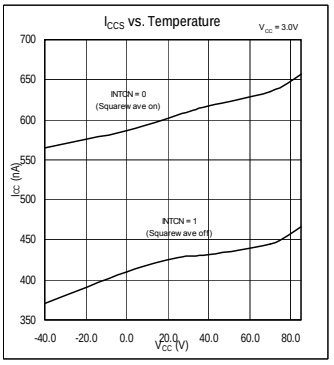
Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF bit to be set over the voltage range of $V_{CC(MIN)} \le V_{CC} \le V_{CC(MAX)}$..

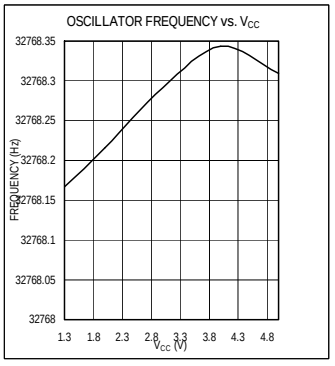
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)





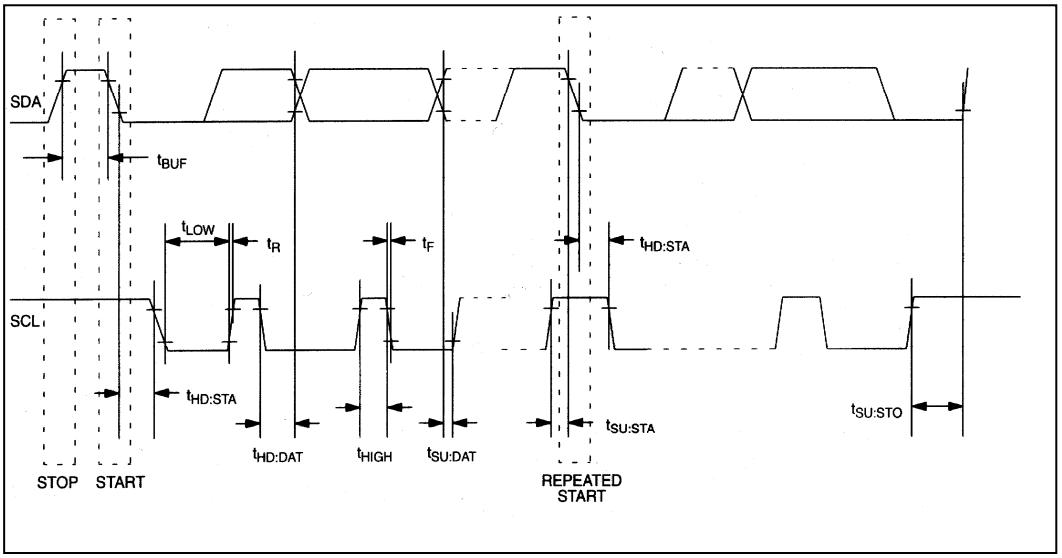




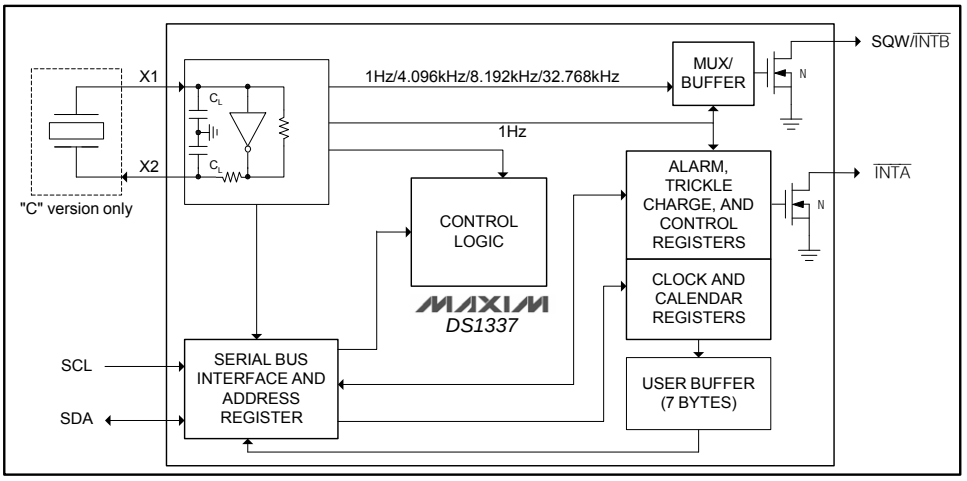
PIN DESCRIPTION

PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. An external 32.768kHz oscillator can also drive the DS1337. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	—	X2	
3	14	$\overline{INTA}$	Interrupt Output. When enabled, $\overline{INTA}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
4	15	GND	Ground. DC power is provided to the device on this pin.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain output and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the serial interface.
7	2	SQW/$\overline{INTB}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
8	3	V_{CC}	DC Power. DC power is provided to the device on this pin.
—	4–13	N.C.	No Connect. These pins are not connected internally, but must be grounded for proper operation.

TIMING DIAGRAM



BLOCK DIAGRAM



DETAILED DESCRIPTION

The *Block Diagram* shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over an I²C bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever V_{CC} is between 5.5V and 1.8V. I²C operation is not guaranteed when V_{CC} is below 1.8V. The DS1337 maintains the time and date when V_{CC} is as low as 1.3V.

OSCILLATOR CIRCUIT

The DS1337 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 1. Crystal Specifications*

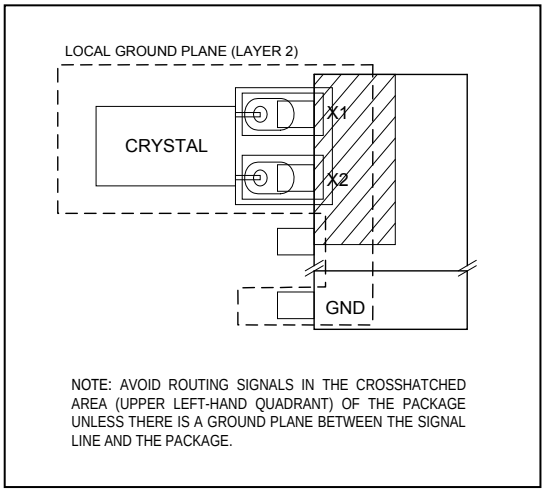
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Figure 1. Typical PC Board Layout for Crystal



DS1337C ONLY

The DS1337C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately +10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

OPERATING MODES

The amount of current consumed by the DS1337 is determined, in part, by the I²C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V_{CC}	Power
I²C Interface Active	1.8V ≤ V_{CC} ≤ 5.5V	I_{CC} Active (I_{CCA})
I²C Interface Inactive	1.8V ≤ V_{CC} ≤ 5.5V	I_{CC} Standby (I_{CCS})
I²C Interface Inactive	1.3V ≤ V_{CC} ≤ 1.8V	Timekeeping (I_{CCTOSC})
I²C Interface Inactive Oscillator Disabled	1.3V ≤ V_{CC} ≤ 1.8V	Data Retention (I_{CCTDDR})

ADDRESS MAP

Table 2 shows the address map for the DS1337 registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Minutes			Minutes				Minutes	00–59
02H	0	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Hours	1–12 +AM/PM 00–23
03H	0	0	0	0	0	Day			Day	1–7
04H	0	0	10 Date		Date				Date	01–31
05H	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06H	10 Year				Year				Year	00–99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09H	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0AH	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	01–31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0CH	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
0DH	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	01–31
0EH	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied or V_{CC} falls below the V_{OSC}.*

I²C INTERFACE

The I²C interface is accessible whenever V_{CC} is at a valid level. If a microcontroller connected to the DS1337 resets while reading from the DS1337 during an I²C read, the two could become unsynchronized. The microcontroller must terminate the last byte read with a Not-Acknowledge (NACK) to properly terminate the read. When the microcontroller resets, the DS1337 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 2. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{\text{AM}}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/$\overline{24}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 3 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{\text{DT}}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/$\overline{\text{DT}}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{\text{DT}}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. The bit(s) will remain at a logic 1 until written to a logic 0 by the user. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$) signals. The match is tested on the once-per-second update of the time and date registers.

Table 3. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQW/$\overline{INTB}$ Output

INTCN	RS2	RS1	SQW/$\overline{INTB}$ OUTPUT	A2IE
0	0	0	1Hz	X
0	0	1	4.096kHz	X
0	1	0	8.192kHz	X
0	1	1	32.768kHz	X
1	X	X	$\overline{A2F}$	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers l activates the $\overline{INTA}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{INTB}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INTB}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INTA}$ (when INTCN = 0) or to assert SQW/$\overline{INTB}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INTA}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{INTA}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} is insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{INTA}$ or SQW/$\overline{INTB}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{INTA}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{INTB}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{INTA}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

I²C SERIAL DATA BUS

The DS1337 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1337 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1337 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

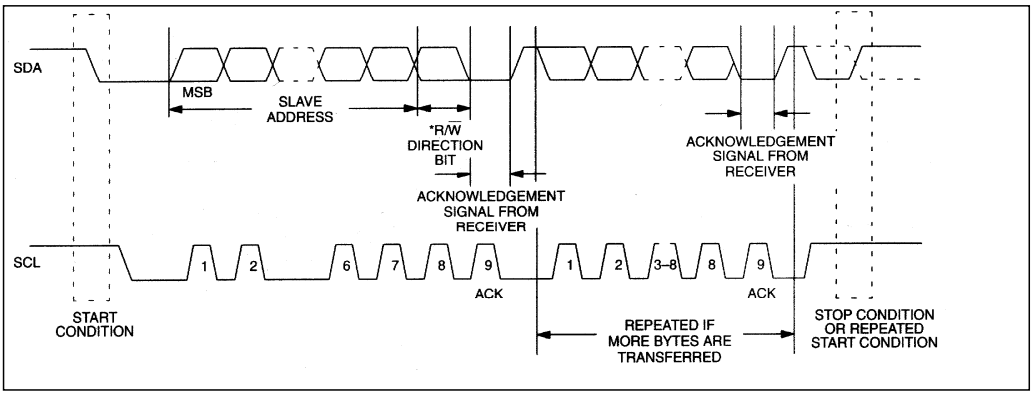
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2. Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1337 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 3). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This sets the register pointer on the DS1337. The master may then transmit zero or more bytes of data, with the DS1337 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 4 and Figure 5). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a “not acknowledge” to end a read.

Figure 3. Data Write—Slave Receiver Mode

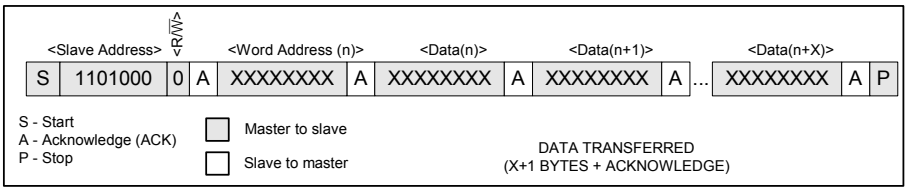


Figure 4. Data Read (from Current Pointer Location)—Slave Transmitter Mode

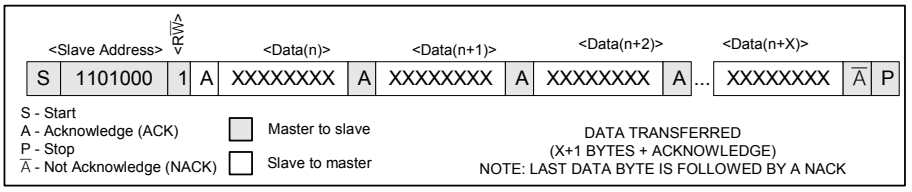
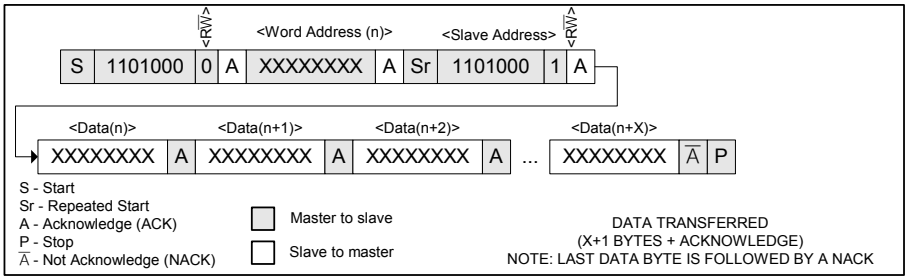


Figure 5. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



HANDLING, PC BOARD LAYOUT, AND ASSEMBLY

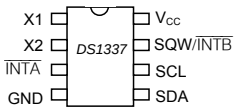
The DS1337C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

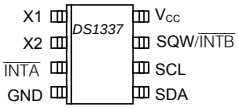
Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

PIN CONFIGURATIONS

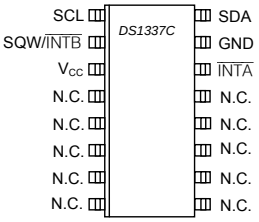
TOP VIEW



DIP



SO, µSOP



SO (300 mils)

CHIP INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL INFORMATION

PACKAGE	THETA-J_A (°C/W)	THETA-J_C (°C/W)
8 DIP	110	40
8 SO	170	40
8 µSOP	229	39
16 SO	73	23

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8+8	**21-0043**
8 SO	S8+2	**21-0041**
8 µMAX	U8+1	**21-0036**
16 SO	W16-H2	**21-0042**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
080508	Added device access details to *General Description* section.	1
	Removed leaded ordering numbers from the *Ordering Information* table.	1
	Added Note 5 to Timekeeping V_{CC} EC table range.	2
	Added “Full Operation” and “Timekeeping” to headers to clarify table usage.	2
	Added OSF parameter to EC table.	3
	Updated *Pin Description* to indicate max input voltage and that unused outputs may be left open.	5
	Added oscillator circuit and show open-drain transistors on *Block Diagram*.	6
	Added *Operating Mode* section with details on operating mode and corresponding Icc parameter.	7
	Added *I²C Interface* section explaining how to synchronize a microcontroller and the RTC.	8
	Corrected legend in figure 5 for not-acknowledge (add overbar to symbol).	14
071609	Removed conflicting SDA/SCL input bias statement in *Pin Description*.	5

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

PRELIMINARY

www.ti.com SBVS083C–JANUARY 2007–REVISED MAY 2008

150mA, Low-Dropout Regulator, Ultralow-Power, I_Q 500nA with Pin-Selectable, Dual-Level Output Voltage

FEATURES

- **Low I_Q: 500nA**
- **150mA, Low-Dropout Regulator with Pin-Selectable Dual Voltage Level Output**
- **Low Dropout: 200mV at 150mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Available in Dual-Level, Fixed Output Voltages from 1.5V to 4.2V Using Innovative Factory EPROM Programming**
- **Available in an Adjustable Version from 1.22V to 5.25V or a Dual-Level Output Version**
- **V_{SET} Pin Toggles Output Voltage Between Two Factory-Programmed Voltage Levels**
- **Stable with a 1.0µF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **CMOS Logic Level-Compatible Enable Pin**
- **Available in DDC (TSOT23-5) or DRV (2mm × 2mm SON-6) Package Options**

APPLICATIONS

- **TI MSP430 Attach Applications**
- **Power Rails with Programming Mode**
- **Dual Voltage Levels for Power-Saving Mode**
- **Wireless Handsets, Smartphones, PDAs, MP3 Players, and Other Battery-Operated Handheld Products**

DESCRIPTION

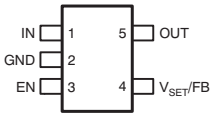
The TPS780 family of low-dropout (LDO) regulators offer the benefits of ultralow power (I_Q = 500nA), miniaturized packaging (2×2 SON-6), and selectable dual-level output voltage levels. An adjustable version is also available, but does not have the capability to shift voltage levels.

The V_{SET} pin allows the end user to switch between two voltage levels *on-the-fly* through a microprocessor-compatible input. This LDO is designed specifically for battery-powered applications where dual-level voltages are needed. With ultralow I_Q (500nA), microprocessors, memory cards, and smoke detectors are ideal applications for this device.

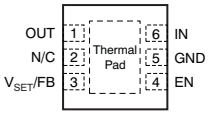
The ultralow-power and selectable dual-level output voltages allow designers to customize power consumption for specific applications. Designers can now shift to a lower voltage level in a battery-powered design when the microprocessor is in sleep mode, further reducing overall system power consumption. The two voltage levels are preset at the factory through a unique architecture using an EPROM. The EPROM technique allows for numerous output voltage options between V_{SET} low (1.5V to 4.2V) and V_{SET} high (2.0V to 3.0V) in the fixed output version only. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

The TPS780 series are designed to be compatible with the TI MSP430 and other similar products. The enable pin is compatible with standard CMOS logic. This LDO is stable with any output capacitor greater than 1.0µF. Therefore, implementations of this device require minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS780 series I_Q (500nA) also come with thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to +125°C. For more cost-sensitive applications requiring a dual-level voltage option and only *on par* I_Q, consider the TPS781 series, with an I_Q of 1.0µA and dynamic voltage scaling.

TPS780DDC
TSOT23-5
(TOP VIEW)



TPS780DRV
2mm x 2mm SON-6
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PRODUCT	V_{OUT}
TPS780**vvvxxxyyyz**	**VVV** is the nominal output voltage for $V_{OUT(HIGH)}$ and corresponds to V_{SET} pin low. **XXX** is the nominal output voltage for $V_{OUT(LOW)}$ and corresponds to V_{SET} pin high. **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250). Adjustable version(3)(4)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Additional output voltage combinations are available on a quick-turn basis using innovative, factory EPROM programming. Minimum-order quantities apply; contact your sales representative for details and availability.
(3) To order the adjustable version, use *TPS78001YYYZ*.
(4) The device is either fixed voltage, dual-level V_{OUT}, or adjustable voltage only. Device design does not permit a fixed and adjustable output simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

PARAMETER		TPS780 Series	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable and V_{SET} voltage range, V_{EN} and V_{VSET}		–0.3 to V_{IN} + 0.3(2)	V
Output voltage range, V_{OUT}		–0.3 to V_{IN} + 0.3V	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See the Dissipation Ratings table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–40 to +125	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} and V_{VSET} absolute maximum rating are V_{IN} + 0.3V or +6.0V, whichever is less.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(1)	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

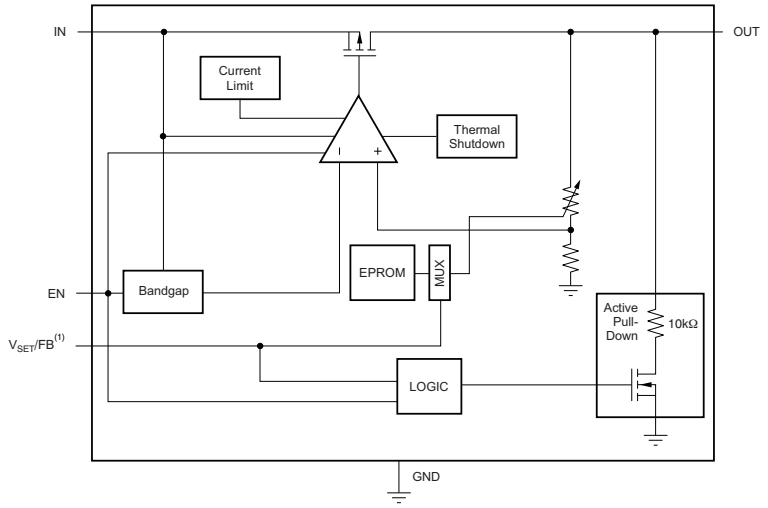
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{VSET} = V_{EN} = V_{IN}, C_{OUT} = 1.0µF, fixed or adjustable, unless otherwise noted. Typical values at T_J = +25°C.

PARAMETER			TEST CONDITIONS		TPS780 Series MIN	TPS780 Series TYP	TPS780 Series MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT}[1]	DC output accuracy	Nominal	T_J = +25°C, V_{SET} = high/low		–2	±1	+2	%
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 150mA, V_{SET} = high/low		–3.0	±2.0	+3.0	%
V_{FB}	Internal reference[2] (adjustable version only)		T_J = +25°C, V_{IN} = 4.0V, I_{OUT} = 75mA			1.216		V
V_{OUT_RANGE}	Output voltage range[3][4] (adjustable version only)		V_{IN} = 5.5V, I_{OUT} = 100µA[2]		V_{FB}	5.25		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 5mA		–1		+1	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 150mA		–2		+2	%
V_{DO}	Dropout voltage[5]		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150mA				250	mV
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 1mA			86		μV_{RMS}
V_{HI}	V_{SET} high (output $V_{OUT(LOW)}$ selected), or EN high (enabled)				1.2		V_{IN}	V
V_{LO}	V_{SET} low (output $V_{OUT(HIGH)}$ selected), or EN low (disabled)				0		0.4	V
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(NOM)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA[6]			420	800	nA
			I_{OUT} = 150mA			5		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.2V ≤ V_{IN} < 5.5V, T_J = –40°C to +100°C			18	130	nA
I_{VSET}	V_{SET} pin current		V_{EN} = V_{VSET} = 5.5V				70	nA
I_{EN}	EN pin current		V_{EN} = V_{VSET} = 5.5V				40	nA
I_{FB}	FB pin current[7] (adjustable version only)		V_{IN} = 5.5V, V_{OUT} = 1.2V, I_{OUT} = 100µA				10	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA	f = 10Hz		40		dB
				f = 100Hz		20		dB
				f = 1kHz		15		dB
$t_{TR(H\rightarrow L)}$	V_{OUT} transition time (high-to-low) V_{OUT} = 97% × $V_{OUT(HIGH)}$		V_{OUT_LOW} = 2.2V, $V_{OUT(HIGH)}$ = 3.3V, I_{OUT} = 10mA			800		µs
$t_{TR(L\rightarrow H)}$	V_{OUT} transition time (low-to-high) V_{OUT} = 97% × $V_{OUT(LOW)}$		V_{OUT_HIGH} = 3.3V, $V_{OUT(LOW)}$ = 2.2V, I_{OUT} = 10mA			800		µs
t_{STR}	Startup time[8]		C_{OUT} = 1.0µF, V_{OUT} = 10% $V_{OUT(NOM)}$ to V_{OUT} = 90% $V_{OUT(NOM)}$			500		µs
t_{SHDN}	Shutdown time[9]		I_{OUT} = 150mA, C_{OUT} = 1.0µF, V_{OUT} = 2.8V, V_{OUT} = 90% $V_{OUT(NOM)}$ to V_{OUT} = 10% $V_{OUT(NOM)}$			500[10]		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			+160		°C
			Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature				–40		+125	°C

(1) The output voltage for V_{SET} = low/high is programmed at the factory.
(2) Adjustable version only.
(3) No V_{SET} pin on the adjustable version.
(4) No dynamic voltage scaling on the adjustable version.
(5) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.3V because minimum V_{IN} = 2.2V.
(6) I_{GND} = 800nA (max) up to +100°C.
(7) The TPS78001 FB pin is tied to V_{OUT}. Adjustable version only.
(8) Time from V_{EN} = 1.2V to V_{OUT} = 90% ($V_{OUT(NOM)}$).
(9) Time from V_{EN} = 0.4V to V_{OUT} = 10% ($V_{OUT(NOM)}$).
(10) See *Shutdown* in the *Application Information* section for more details.

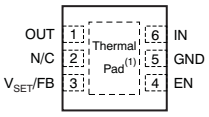
FUNCTIONAL BLOCK DIAGRAM



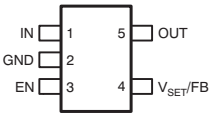
(1) Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions.

PIN CONFIGURATIONS

TPS780DRV
2mm x 2mm SON-6
(TOP VIEW)



TPS780DDC
TSOT23-5
(TOP VIEW)



(1) It is recommended that the SON package thermal pad be connected to ground.

Table 1. TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	DRV	DDC	
OUT	1	5	Regulated output voltage pin. A small (1µF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the Application Information section for more details.
N/C	2	—	Not connected.
V_{SET}/FB	3	4	Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions. Driving the select pin (V_{SET}) below 0.4V selects preset output voltage high. Driving the V_{SET} pin over 1.2V selects preset output voltage low.
EN	4	3	Driving the enable pin (EN) over 1.2V turns on the regulator. Driving this pin below 0.4V puts the regulator into shutdown mode, reducing operating current to 18nA typical.
GND	5	2	Ground pin.
IN	6	1	Input pin. A small capacitor is needed from this pin to ground to assure stability. Typical input capacitor = 1.0µF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
Thermal pad	Thermal pad	—	It is recommended that the SON package thermal pad be connected to ground.

TYPICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 1.22V (typ)
TPS78001

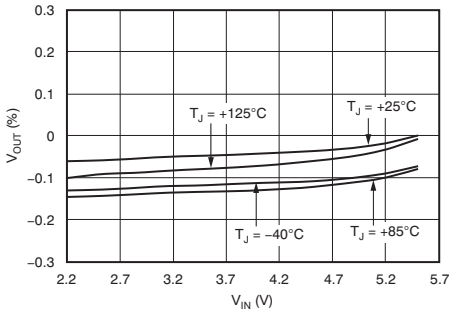


Figure 1.

LINE REGULATION
I_{OUT} = 5mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V (typ)
TPS780330220

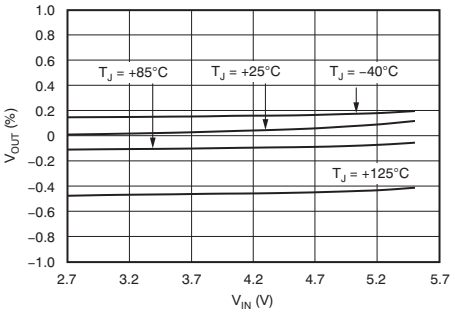


Figure 2.

LINE REGULATION
I_{OUT} = 150mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V (typ)
TPS780330220

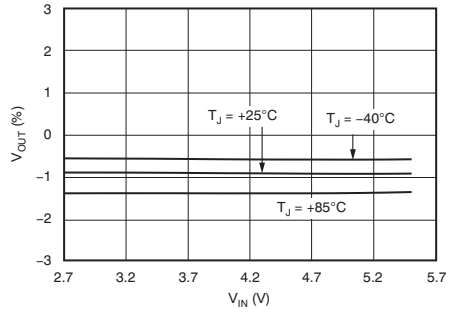


Figure 3.

LINE REGULATION
I_{OUT} = 5mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ)
TPS780330220

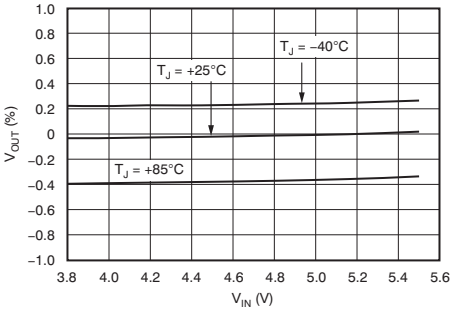


Figure 4.

LINE REGULATION
I_{OUT} = 150mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ)
TPS780330220

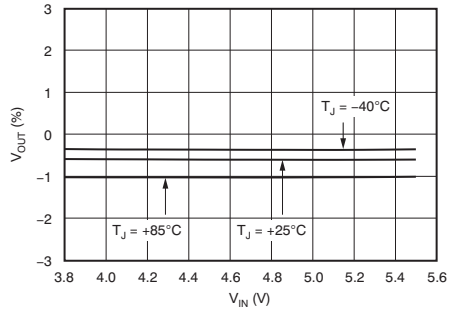


Figure 5.

LOAD REGULATION
V_{OUT} = 3.3V
TPS78001

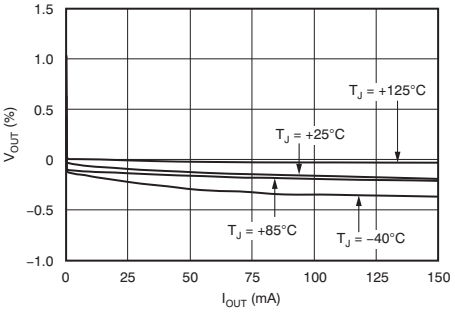


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

LOAD REGULATION
V_{VSET} = 1.2V, V_{IN} = 2.7V, V_{OUT} = 2.2V
TPS780330220

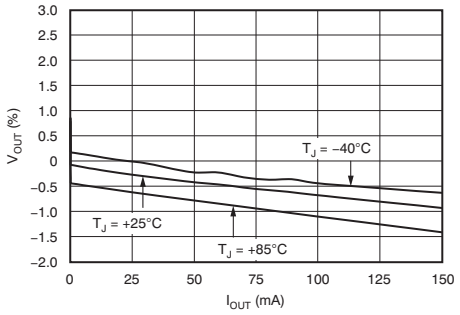


Figure 7.

LOAD REGULATION
V_{VSET} = 0.4V, V_{IN} = 3.8V, V_{OUT} = 3.3V
TPS780330220

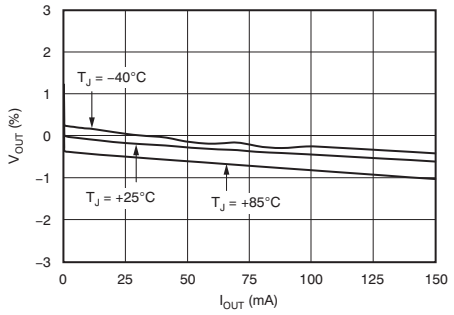


Figure 8.

DROPOUT VOLTAGE vs OUTPUT CURRENT
V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78001

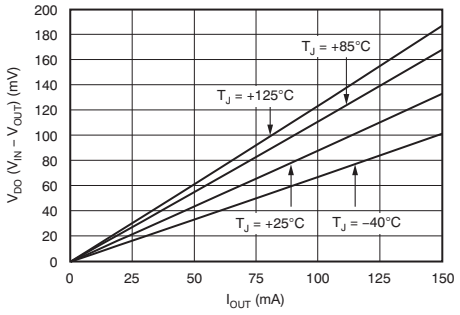


Figure 9.

DROPOUT VOLTAGE vs OUTPUT CURRENT
V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS780330220

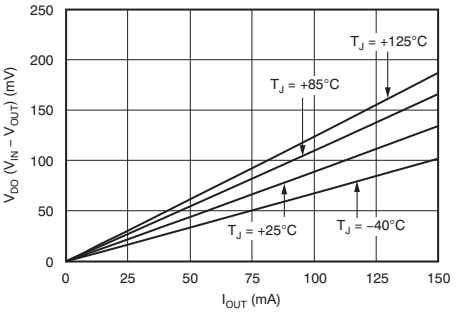


Figure 10.

DROPOUT VOLTAGE vs TEMPERATURE
V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78001

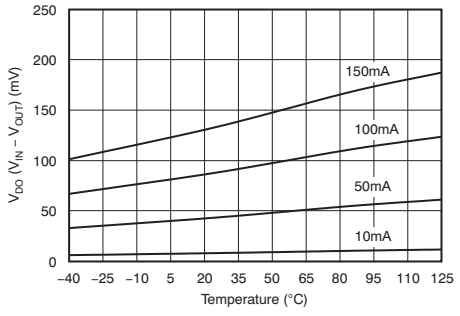


Figure 11.

DROPOUT VOLTAGE vs TEMPERATURE
V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS780330220

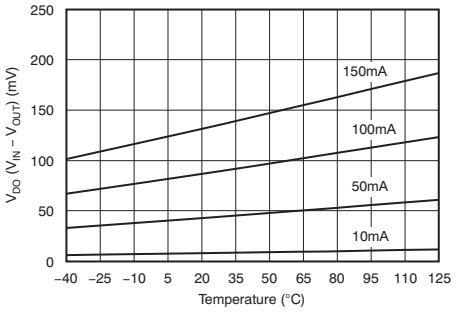


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{OUT} = 1.22V
TPS78001

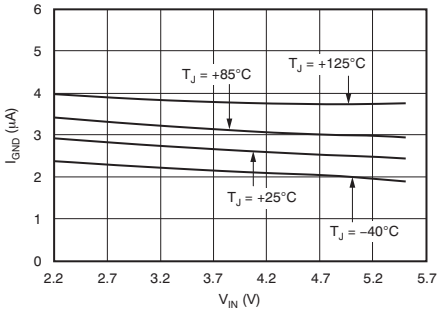


Figure 13.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{OUT} = 1.22V
TPS78001

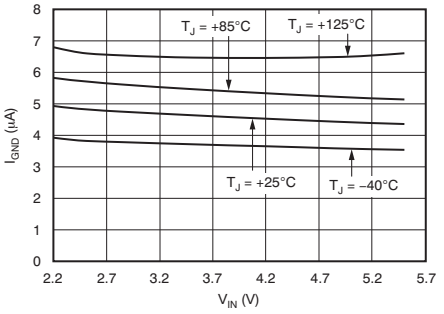


Figure 14.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 0mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

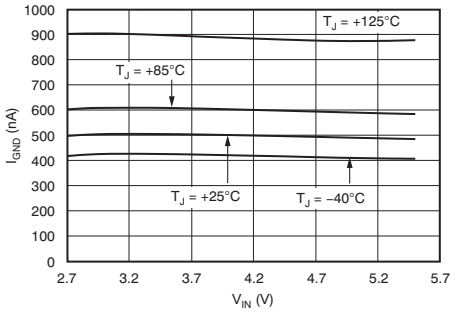


Figure 15.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 1mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

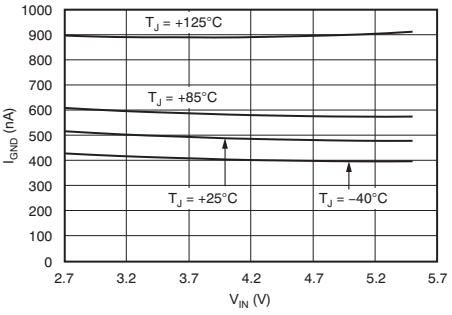


Figure 16.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

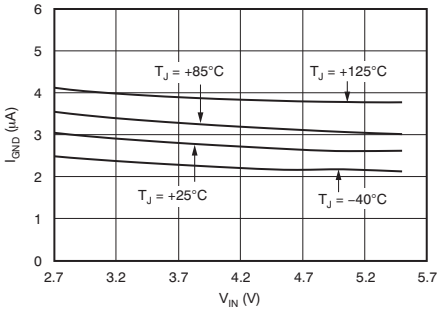


Figure 17.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

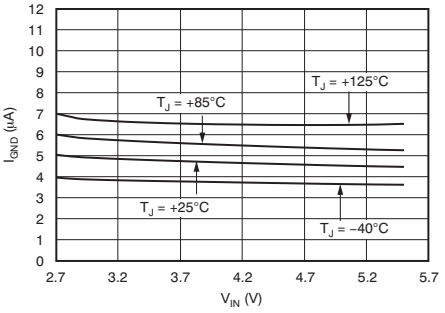


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 0mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

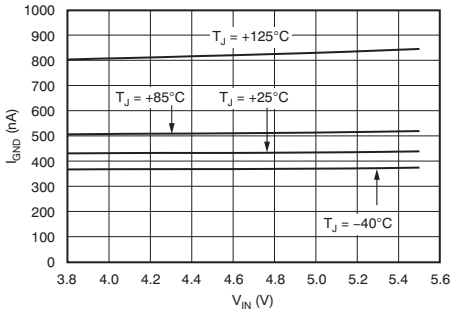


Figure 19.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 1mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

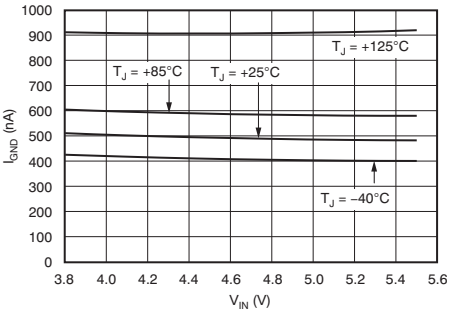


Figure 20.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

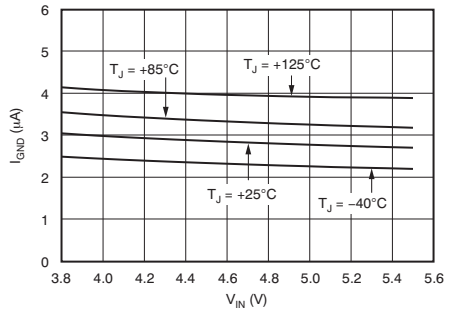


Figure 21.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

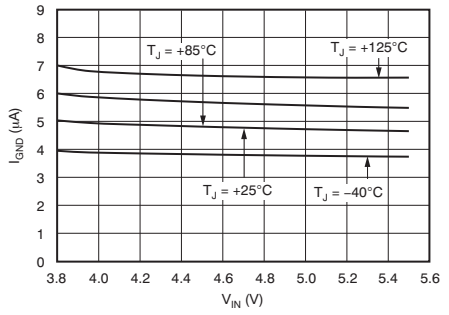


Figure 22.

GROUND PIN CURRENT vs OUTPUT CURRENT
V_{VSET} = 1.2V, V_{IN} = 5.5V, V_{OUT} = 2.2V
TPS780330220

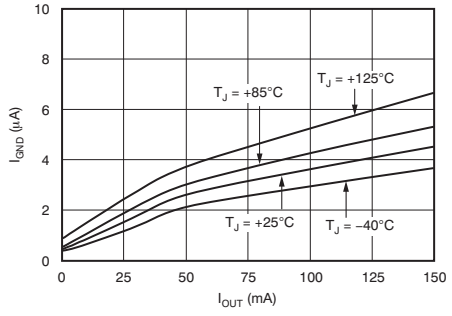


Figure 23.

GROUND PIN CURRENT vs OUTPUT CURRENT
V_{VSET} = 0.4V, V_{IN} = 5.5V, V_{OUT} = 3.3V
TPS780330220

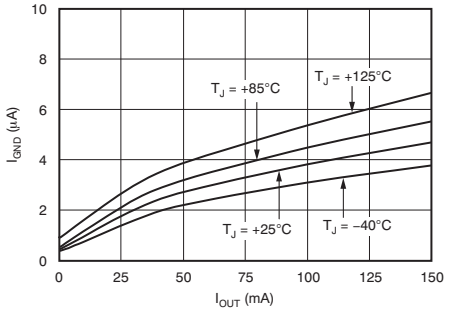


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

SHUTDOWN CURRENT vs INPUT VOLTAGE
I_{OUT} = 0mA, V_{VSET} = 0.4V
TPS78001

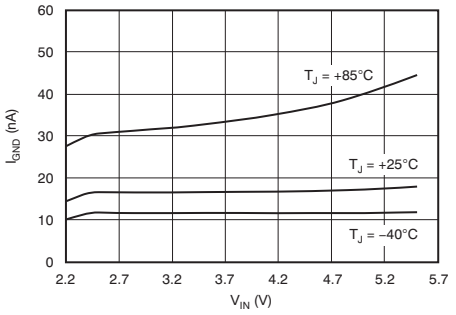


Figure 25.

CURRENT LIMIT vs INPUT VOLTAGE
V_{OUT} = 90% V_{OUT} (typ), V_{OUT} = 1.22V (typ)
TPS78001

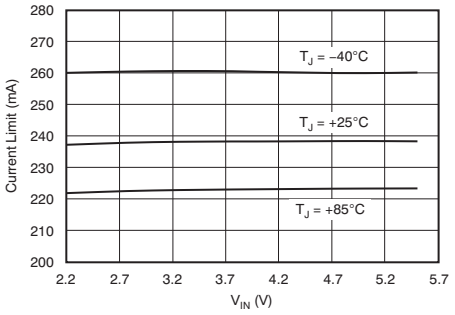


Figure 26.

CURRENT LIMIT vs INPUT VOLTAGE
V_{VSET} = 1.2V, V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 2.2V (typ)
TPS780330220

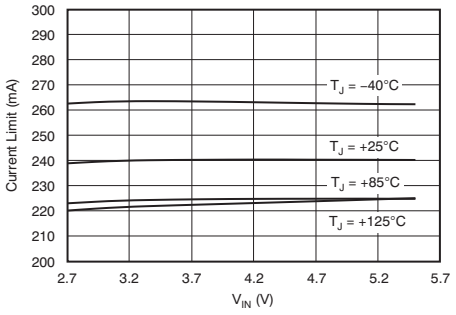


Figure 27.

CURRENT LIMIT vs INPUT VOLTAGE
V_{VSET} = 0.4V, V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 3.3V (typ)
TPS780330220

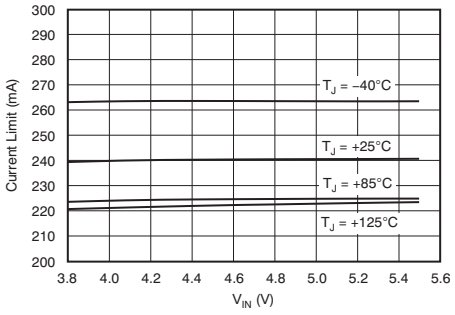


Figure 28.

FEEDBACK PIN CURRENT vs TEMPERATURE
I_{OUT} = 0mA, V_{OUT} = 1.22V
TPS78001

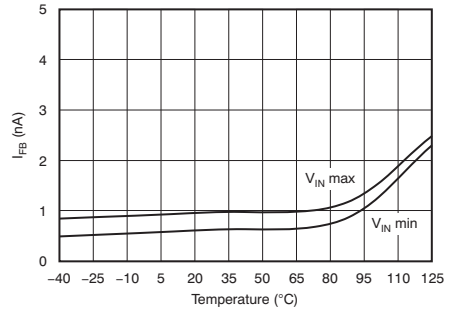


Figure 29.

V_{SET} PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

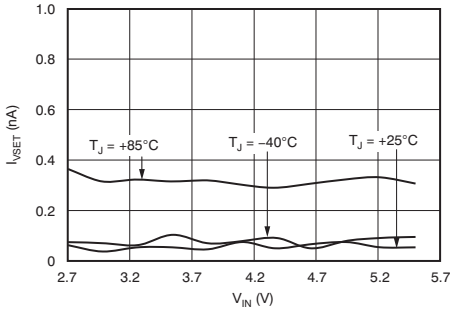


Figure 30.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

V_{SET} PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

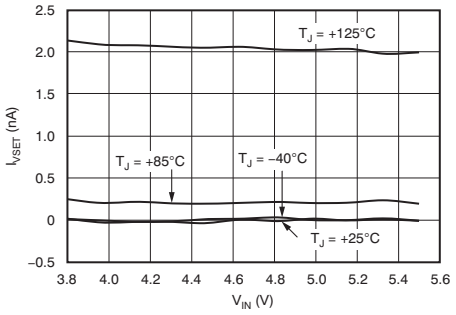


Figure 31.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 1mA, V_{OUT} = 1.22V
TPS78001

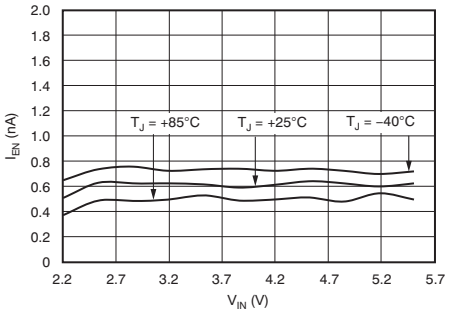


Figure 32.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS780330220

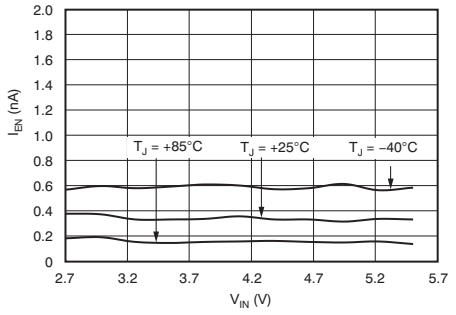


Figure 33.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS780330220

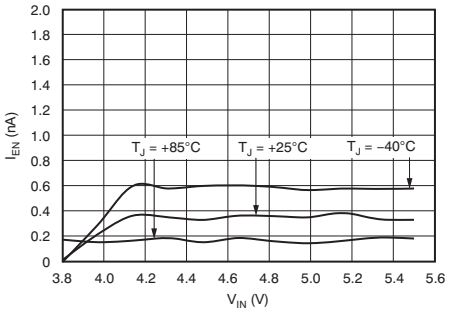


Figure 34.

ENABLE PIN HYSTERESIS vs TEMPERATURE
I_{OUT} = 1mA, TPS78001

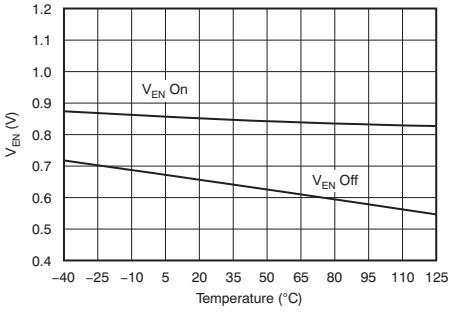


Figure 35.

ENABLE PIN HYSTERESIS vs TEMPERATURE
I_{OUT} = 1mA, TPS780330220

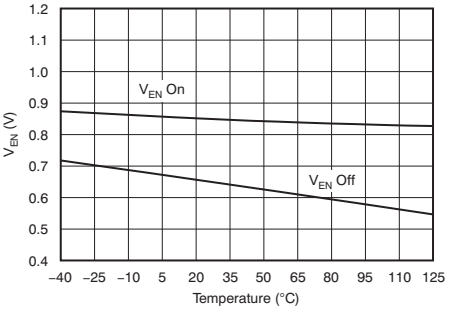


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

%ΔV$_{OUT}$ vs TEMPERATURE
I$_{OUT}$ = 1mA, V$_{IN}$ = 3.8V, V$_{OUT}$ = 3.3V
TPS78001

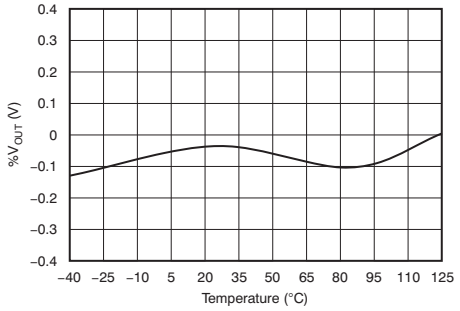


Figure 37.

%ΔV$_{OUT}$ vs TEMPERATURE
V$_{VSET}$ = 1.2V, V$_{IN}$ = 2.7V, V$_{OUT}$ = 2.2V (typ)
TPS780330220

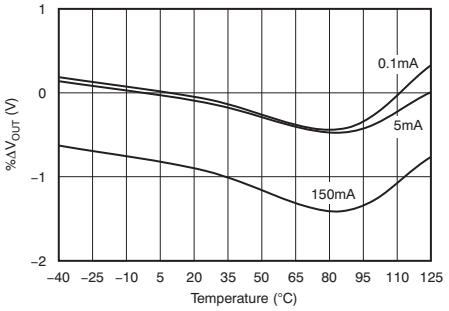


Figure 38.

%ΔV$_{OUT}$ vs TEMPERATURE
V$_{VSET}$ = 0.4V, V$_{IN}$ = 3.8V, V$_{OUT}$ = 3.3V (typ)
TPS780330220

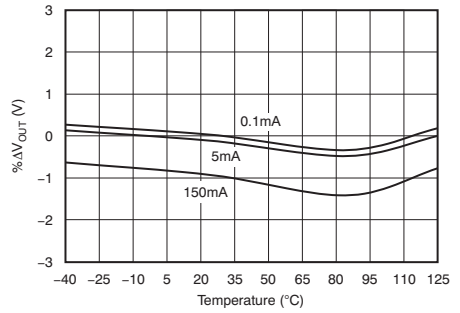


Figure 39.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY
C$_{IN}$ = 1µF, C$_{OUT}$ = 2.2µF, V$_{VSET}$ = 1.2V, V$_{IN}$ = 2.7V
TPS780330220

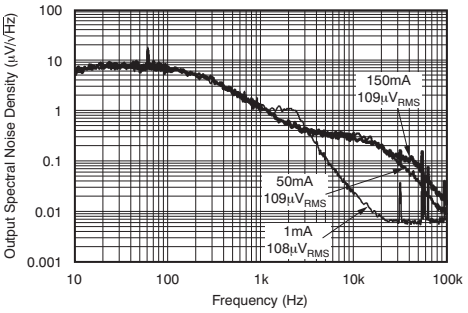


Figure 40.

RIPPLE REJECTION vs FREQUENCY
V$_{IN}$ = 2.7V, V$_{OUT}$ = 1.2V, C$_{OUT}$ = 2.2µF
TPS78001

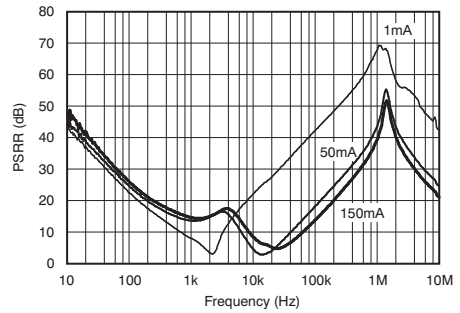


Figure 41.

INPUT VOLTAGE RAMP vs OUTPUT VOLTAGE
TPS780330220

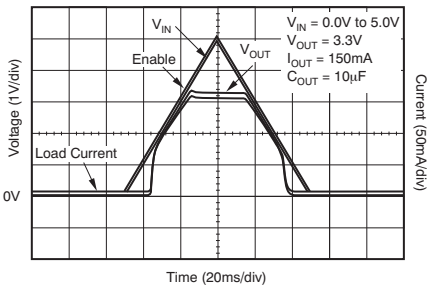


Figure 42.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

OUTPUT VOLTAGE vs ENABLE (SLOW RAMP)
TPS780330220

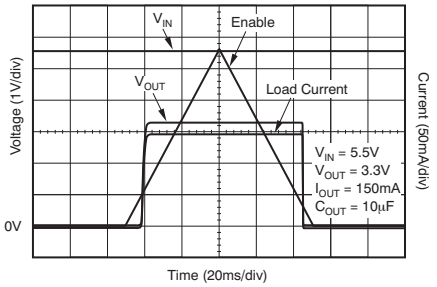


Figure 43.

INPUT VOLTAGE vs DELAY TO OUTPUT
TPS780330220

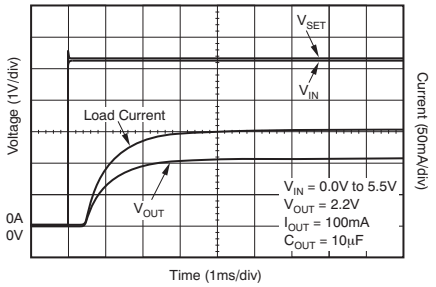


Figure 44.

LINE TRANSIENT RESPONSE
TPS780330220

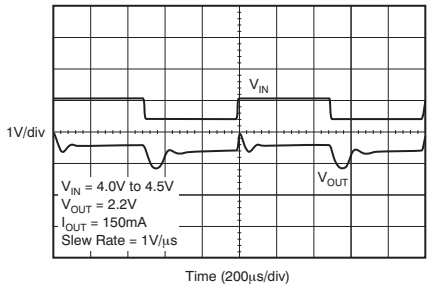


Figure 45.

LINE TRANSIENT RESPONSE
TPS780330220

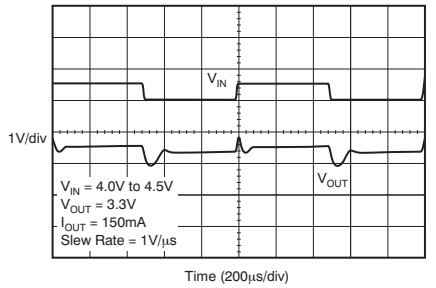


Figure 46.

LOAD TRANSIENT RESPONSE
TPS780330220

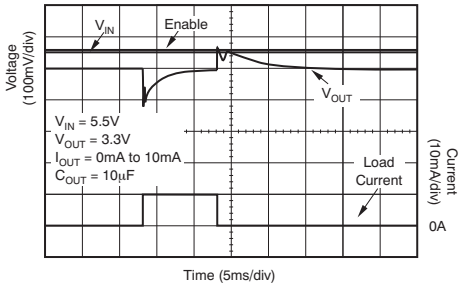


Figure 47.

LOAD TRANSIENT RESPONSE
TPS780330220

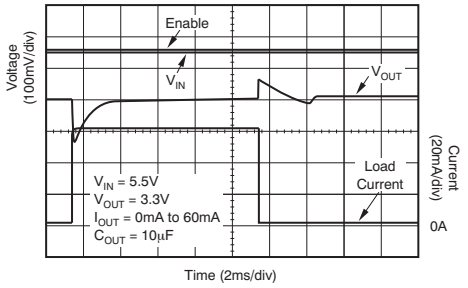


Figure 48.

PRELIMINARY

19-0275; Rev 4; 7/09

MAXIM

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

General Description

The MAX882/MAX883/MAX884 linear regulators maximize battery life by combining ultra-low supply currents and low dropout voltages. They feature 200mA output current capability at up to +125°C junction temperature and come in a 1.5W SOIC package. The 1.5W package (compared to 0.47W for standard SOIC packages) allows a wider operating range for the input voltage and output current. The MAX882/MAX883/MAX884 use a p-channel MOSFET pass transistor to maintain a low 11µA (15µA max) supply current from no-load to the full 200mA output. Unlike earlier bipolar regulators, there are no PNP base current losses that increase with output current. In dropout, the MOSFET does not suffer from excessive base currents that occur when PNP transistors go into saturation. Typical dropout voltages are 220mV at 5V and 200mA, or 320mV at 3.3V and 200mA.

The MAX882 features a 7µA standby mode that disables the output but keeps the reference, low-battery comparator, and biasing circuitry alive. The MAX883/MAX884 feature a shutdown (OFF) mode that turns off all circuitry, reducing supply current to less than 1µA. All three devices include a low-battery-detection comparator, foldback current limiting, reverse-current protection, and thermal-overload protection.

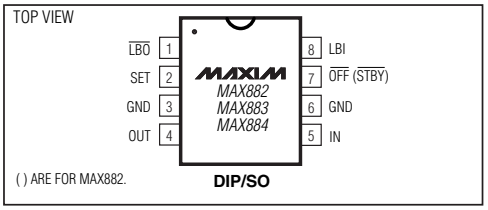
The output is preset at 3.3V for the MAX882/MAX884 and 5V for the MAX883. In addition, all devices employ Dual Mode™ operation, allowing user-adjustable outputs from 1.25V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

For low-dropout linear regulators with output currents up to 500mA, refer to the MAX603/MAX604 data sheet.

Applications

Pagers and Cellular Phones
3.3V and 5V Regulators
1.25V to 11V Adjustable Regulators
High-Efficiency Linear Regulators
Battery-Powered Devices
Portable Instruments
Solar-Powered Instruments

Pin Configuration



Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- **Foldback Current Limiting**
- **High-Power (1.5W) 8-Pin SO Package**
- **Dual Mode Operation: Fixed or Adjustable Output from 1.25V to 11V**
- **Large Input Range (2.7V to 11.5V)**
- **Internal 1.1Ω p-Channel Pass Transistor Draws No Base Current**
- **Low 220mV Dropout Voltage at 200mA Output Current**
- **11µA (typ) Quiescent Current**
- **1µA (max) Shutdown Mode or 7µA (typ) Standby Mode**
- **Low-Battery Detection Comparator**
- **Reverse-Current Protection**
- **Thermal-Overload Protection**

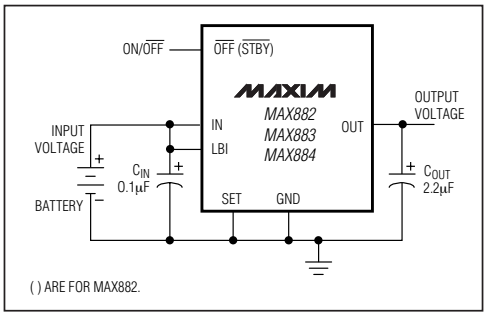
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX882CPA	0°C to +70°C	8 PDIP
MAX882CSA	0°C to +70°C	8 SO
MAX882C/D	0°C to +70°C	Dice*
MAX882EPA	-40°C to +85°C	8 PDIP
MAX882ESA	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

**Dice are tested at T_J = +25°C, DC parameters only.*
***Contact factory for availability.*

Typical Operating Circuit



5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN or OUT to GND).....-0.3V to +12V
Output Short-Circuit Duration 1min
Continuous Output Current 300mA
$\overline{LBO}$ Output Current 50mA
$\overline{LBO}$ Output Voltage and LBI,
SET, STBY, OFF Input Voltages .....-0.3V to the greater of (IN + 0.3V) or (OUT + 0.3V)
Continuous Power Dissipation (T_J = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
High-Power SO (derate 18.75mW/°C above +70°C).....1.5W
CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX88_C_A.....0°C to +70°C
MAX88_E_A.....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 6V (MAX883) or V_{IN} = 4.3V (MAX882/MAX884), C_{OUT} = 2.2µF, STBY or OFF = V_{IN}, SET = GND, LBI = V_{IN}, T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	SET = OUT, R_L = 1kΩ	MAX88_C_A	2.7		11.5	V
			MAX88_E_A	2.9		11.5	
			MAX88_MJA	3.0		11.5	
Output Voltage (Note 2)	V_{OUT}	MAX883, 6.0V ≤ V_{IN} ≤ 11.5V	I_{OUT} = 100µA - 250mA, 0°C ≤ T_J ≤ +85°C	4.75	5.00	5.25	V
			I_{OUT} = 100µA - 250mA, -40°C ≤ T_J ≤ +85°C	4.65		5.35	
		MAX882/MAX884, 4.3V ≤ V_{IN} ≤ 11.5V	I_{OUT} = 100µA - 200mA, 0°C ≤ T_J ≤ +85°C	3.15	3.30	3.45	
			I_{OUT} = 100µA - 200mA, -40°C ≤ T_J ≤ +85°C	3.07		3.53	
Load Regulation	ΔV_{LDR}	I_{OUT} = 1mA to 200mA	MAX883C_A/E_A		60	100	mV
			MAX883MJA			150	
		I_{OUT} = 1mA to 150mA	MAX882, MAX884		30	100	
Line Regulation	ΔV_{LNR}	(V_{OUT} + 0.5V) < V_{IN} < 11.5V, I_{OUT} = 10mA			10	40	mV
Dropout Voltage (Note 3)	ΔV_{DO}	MAX883	I_{OUT} = 100mA		110	220	mV
			I_{OUT} = 200mA		220	440	
		MAX882/MAX884	I_{OUT} = 100mA		160	320	
			I_{OUT} = 200mA		320	640	
Quiescent Current	I_Q	SET = OUT, V_{IN} = 6V	MAX88_C_A/E_A		11	15	µA
			MAX88_MJA			30	
		V_{IN} = 11.5V	MAX88_C_A/E_A		15	25	
			MAX88_MJA			40	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 6V (MAX883) or V_{IN} = 4.3V (MAX882/MAX884), C_{OUT} = 2.2µF, STBY or OFF = V_{IN}, SET = GND, LBI = V_{IN}, T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STBY Quiescent Current (Note 4)	$I_{Q\ STBY}$	STBY = 0, V_{IN} = 6V, SET = OUT	MAX882C_A/E_A		7	15	µA
			MAX882MJA			30	
		STBY = 0, V_{IN} = 11.5V, SET = OUT	MAX882C_A/E_A		10	25	
			MAX882MJA			40	
OFF Quiescent Current	$I_{Q\ OFF}$	OFF = 0, R_L = 1kΩ, V_{IN} = 11.5V MAX883/MAX884	MAX88_C_A		0.01	1	µA
			MAX88_E_A			5	
			MAX88_MJA			10	
Minimum Load Current	$I_{OUT(MIN)}$	V_{IN} = 11.5V, SET = OUT	MAX88_C_A			1	µA
			MAX88_E_A			3	
			MAX88_MJA			10	
Foldback Current Limit (Note 5)	ILIM	V_{OUT} < 0.8V			170		mA
		V_{OUT} > 0.8V and V_{IN} - V_{OUT} > 0.7V			430		
Thermal Shutdown Temperature	T_{SD}				+160		°C
Thermal Shutdown Hysteresis	ΔT_{SD}				10		°C
Reverse-Current-Protection (Note 6)	ΔV_{RTH}	V_{OUT} = 4.5V	MAX883_A		6	20	mV
		V_{OUT} = 3.0V	MAX882_A, MAX884_A		6	20	
Reverse Leakage Current	I_{RVL}	MAX882: V_{IN} = 0, STBY = 0, V_{OUT} = 3.0V			7		µA
		MAX883/MAX884: V_{IN} = 0, OFF = 0, V_{OUT} = 3.0V			0.01		
Startup Overshoot	V_{OSH}	R_L = 1kΩ, C_{OUT} = 2.2µF					% of V_{OUT}
Time Required to Exit OFF or STBY Modes	T_{START}	V_{IN} = 9V, R_L = 33Ω, OFF from 0 to V_{IN}, 0% to 95% of V_{OUT}			200		µs
Dual Mode SET Threshold	$V_{SET\ TH}$	For internal feedback			65	30	mV
		For external feedback		150	65		
SET Reference Voltage	V_{SET}	SET = OUT, R_L = 1kΩ	0°C ≤ T_J ≤ +85°C	1.16	1.20	1.24	V
			-40°C ≤ T_J ≤ +85°C	1.12		1.28	
SET Input Leakage Current	I_{SET}	V_{SET} = 1.5V or 0			±0.01	±50	nA
LBI Threshold Voltage	V_{LBI}	LBI signal falling	0°C ≤ T_J ≤ +85°C	1.15	1.20	1.25	V
			-40°C ≤ T_J ≤ +85°C	1.11		1.29	
LBI Hysteresis	ΔV_{LBI}				7		mV
LBI Input Leakage Current	I_{LBI}	V_{LBI} = 1.5V			±0.01	±50	nA
$\overline{LBO}$ Output Low Voltage	$V_{\overline{LBOL}}$	$I_{\overline{LBO}}$ sink = 1.2mA, V_{LBI} = 1V, 3V < V_{IN} < 11.5V, SET = OUT			90	250	mV
$\overline{LBO}$ Output Leakage Current	$I_{\overline{BLO}\ LKG}$	V_{LBI} = V_{IN}, V_{LBO} = V_{IN}			0.01	0.1	µA
OUT Leakage Current	$I_{OUT\ LKG}$	V_{IN} = 11.5V, V_{OUT} = 2V, SET = OUT	MAX88_C_A		0.01	1	µA
			MAX88_E_A			3	
			MAX88_MJA			10	

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 6V (MAX883) or V_{IN} = 4.3V (MAX882/MAX884), C_{OUT} = 2.2µF, STBY or OFF = V_{IN}, SET = GND, LBI = V_{IN}, T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STBY Threshold Voltage	V_{STBY}	STBY signal falling, MAX882_A	1.15	1.20	1.25	V
STBY Hysteresis	ΔV_{STBY}	MAX882_A		7		mV
STBY Input Leakage Current	I_{STBY}	V_{STBY} = V_{IN} or 0, MAX882_A		±0.01	±50	nA
OFF Threshold Voltage	$V_{IL\ OFF}$	In off mode, MAX883_A, MAX884_A			0.4	V
	$V_{IH\ OFF}$	In on mode, SET = OUT, V_{IN} < 6V, MAX883_A, MAX884_A	2.0			
		In on mode, SET = OUT, 6V < V_{IN} < 11.5V, MAX883_A, MAX884_A	3.0			
OFF Input Leakage Current	I_{OFF}	V_{OFF} = V_{IN} or 0		±0.01	±50	nA
Output Noise	e_n	10Hz to 10kHz, SET = OUT, R_L = 1kΩ, C_{OUT} = 2.2µF (Note 7)		250		μV_{RMS}

Note 1: Electrical specifications are measured by pulse testing and are guaranteed for a junction temperature (T_J) within the operating temperature range, unless otherwise noted. Specifications to -40°C are guaranteed by design and not production tested.

Note 2: (V_{IN} - V_{OUT}) is limited to keep the product (I_{OUT} x (V_{IN} - V_{OUT})) from exceeding the package power dissipation limits. See Figure 5. Therefore, the combination of high output current and high supply voltage is not tested.

Note 3: Dropout Voltage is (V_{IN} - V_{OUT}) when V_{OUT} falls to 100mV below its nominal value at V_{IN} = (V_{OUT} + 2V). For example, the MAX883 is tested by measuring the V_{OUT} at V_{IN} = 7V, then V_{IN} is lowered until V_{OUT} falls 100mV below the measured value. The difference (V_{IN} - V_{OUT}) is then measured and defined as ΔV_{DO}.

Note 4: Since standby mode inhibits the output but keeps all biasing circuitry alive, the Standby Quiescent Current is similar to the normal operating quiescent current.

Note 5: Foldback Current Limit was characterized by pulse testing to remain below the maximum junction temperature (not production tested).

Note 6: The Reverse-Current Protection Threshold is the output/input differential voltage (V_{OUT} - V_{IN}) at which reverse-current protection switchover occurs and the pass transistor is turned off. See the section *Reverse-Current Protection* in the *Detailed Description*.

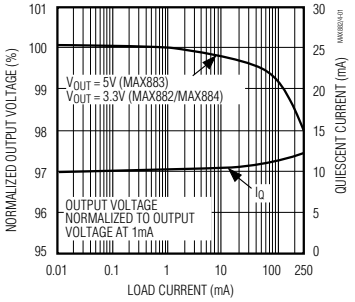
Note 7: Noise is tested using a bandpass amplifier with two poles at 10Hz and two poles at 10kHz.

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

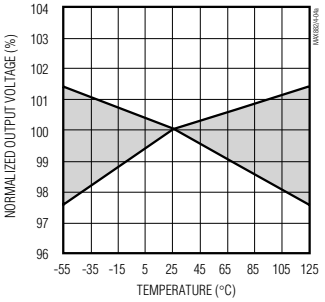
Typical Operating Characteristics

(V_{IN} = 7V for MAX883, V_{IN} = 5.3V for MAX882/MAX884, OFF or STBY = V_{IN}, SET = GND, LBI = V_{IN}, $\overline{LBO}$ = OPEN, C_{IN} = C_{OUT} = 2.2µF, R_L = 1kΩ, T_A = +25°C, unless otherwise noted.)

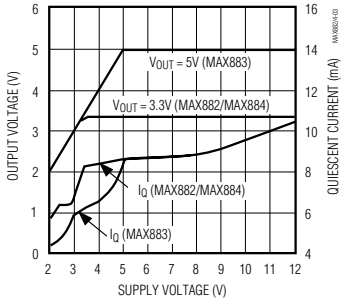
OUTPUT VOLTAGE AND QUIESCENT CURRENT vs. LOAD CURRENT



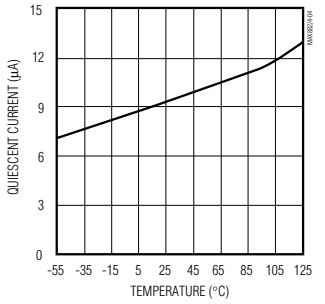
OUTPUT VOLTAGE vs. TEMPERATURE



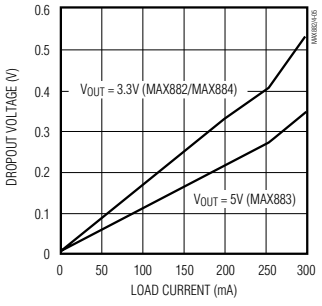
OUTPUT VOLTAGE AND QUIESCENT CURRENT vs. SUPPLY VOLTAGE



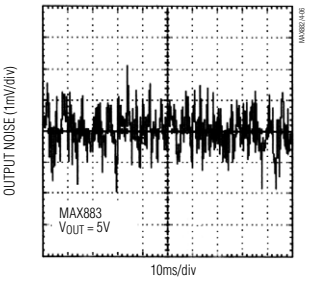
QUIESCENT CURRENT vs. TEMPERATURE



DROPOUT VOLTAGE vs. LOAD CURRENT



10Hz to 10kHz OUTPUT NOISE



5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

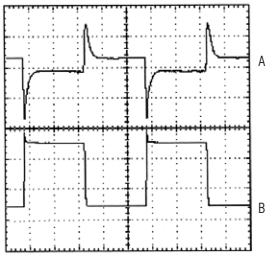
Typical Operating Characteristics (continued)

(V_{IN} = 7V for MAX883, V_{IN} = 5.3V for MAX882/MAX884, OFF or STBY = V_{IN}, SET = GND, LBI = V_{IN}, $\overline{LBO}$ = OPEN, C_{IN} = C_{OUT} = 2.2µF, R_L = 1kΩ, T_A = +25°C, unless otherwise noted.)

LINE-TRANSIENT RESPONSE

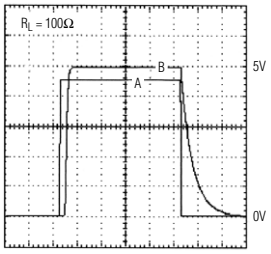
MAX883: V_{OUT} = 5V, C_{IN} = 0µF, t_R = 15µs, t_F = 13µs
A: V_{IN} = 8V (HIGH) / V_{IN} = 7V (LOW)
B: OUTPUT VOLTAGE (100mV/div)

LOAD-TRANSIENT RESPONSE



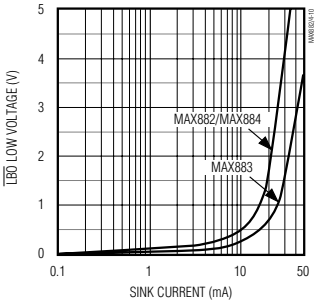
MAX883: V_{OUT} = 5V, t_R = 24µs, t_F = 44µs
A: OUTPUT VOLTAGE (100mV/div)
B: I_{OUT} = 250mA (HIGH) / I_{OUT} = 50mA (LOW)

OVERSHOOT AND TIME EXITING SHUTDOWN MODE



A: $\overline{OFF}$ PIN VOLTAGE (1V/div):
RISE TIME = 9µs
B: MAX883 OUTPUT VOLTAGE (1V/div):
DELAY = 135µs, RISE TIME = 67µs,
OVERSHOOT = 0%

$\overline{LBO}$ LOW VOLTAGE vs. SINK CURRENT



Pin Description

PIN		NAME	DESCRIPTION
MAX882	MAX883/ MAX884		
1	1	$\overline{LBO}$	Low-Battery Output is an open-drain output that goes low when LBI is less than 1.2V. Connect to IN or OUT through a pull-up resistor. $\overline{LBO}$ is undefined during shutdown mode (MAX883/MAX884).
2	2	SET	Feedback for setting the output voltage. Connect to GND to set the output voltage to the preselected 3.3V or 5V. Connect to an external resistor network for adjustable-output operation.
3, 6	3, 6	GND	Ground pins—also function as heatsinks in the SO package. All GND pins must be soldered to the PC board for proper power dissipation. Connect to large copper pads or planes to channel heat from the IC.
4	4	OUT	Regulator Output. Fixed or adjustable from 1.25V to 11.0V. Sources up to 200mA. Bypass with a 2.2µF capacitor.
5	5	IN	Regulator Input. Supply voltage can range from 2.7V to 11.5V.
7	—	STBY	Standby. Active-low comparator input. Connect to GND to disable the output or to IN for normal operation. A resistor network (from IN) can be used to set a standby mode threshold.
—	7	OFF	Shutdown. Active-low logic input. In OFF mode, supply current is reduced below 1µA and V_{OUT} = 0.
8	8	LBI	Low-Battery comparator Input. Tie to IN when not used.

Detailed Description

The MAX882/MAX883/MAX884 are micropower, low-dropout linear regulators designed primarily for battery-powered applications. They feature Dual Mode operation, allowing a fixed output of 5V for the MAX883 and 3.3V for the MAX882/MAX884, or an adjustable output from 1.25V to 11V. These devices supply up to 200mA while requiring less than 15µA quiescent current. As illustrated in Figure 1, they consist of a 1.20V reference, error amplifier, MOSFET driver, p-channel pass transistor, dual-mode comparator, and feedback voltage-divider.

The 1.20V reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the p-channel pass transistor. If the feedback voltage is lower than the reference, the pass transistor's gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage-divider connected to the OUT pin, or an external resistor network connected to the SET pin. The dual-mode comparator examines the SET pin voltage and selects the feedback path used. If the SET pin is below 65mV, internal feedback is used and the output voltage is regulated to 5V for the MAX883 or 3.3V for the MAX882/MAX884. Additional blocks include a foldback current limiter, reverse-current protection, a thermal sensor, shutdown or standby logic, and a low-battery-detection comparator.

Internal p-Channel Pass Transistor

The MAX882/MAX883/MAX884 feature a 200mA P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The p-channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP-based regulators waste large amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX882/MAX883/MAX884 do not suffer from these problems and consume only 11µA of quiescent current during light loads, heavy loads, and dropout.

Output Voltage Selection

The MAX882/MAX883/MAX884 feature Dual Mode operation. In preset voltage mode, the MAX883's output is set to 5V and the MAX882/MAX884's output is set to 3.3V, using internal trimmed feedback resistors. Select this mode by connecting SET to ground.

In preset voltage mode, impedances between SET and ground should be less than 100kΩ. Otherwise, spurious conditions could cause the voltage at SET to exceed the 65mV dual-mode threshold.

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

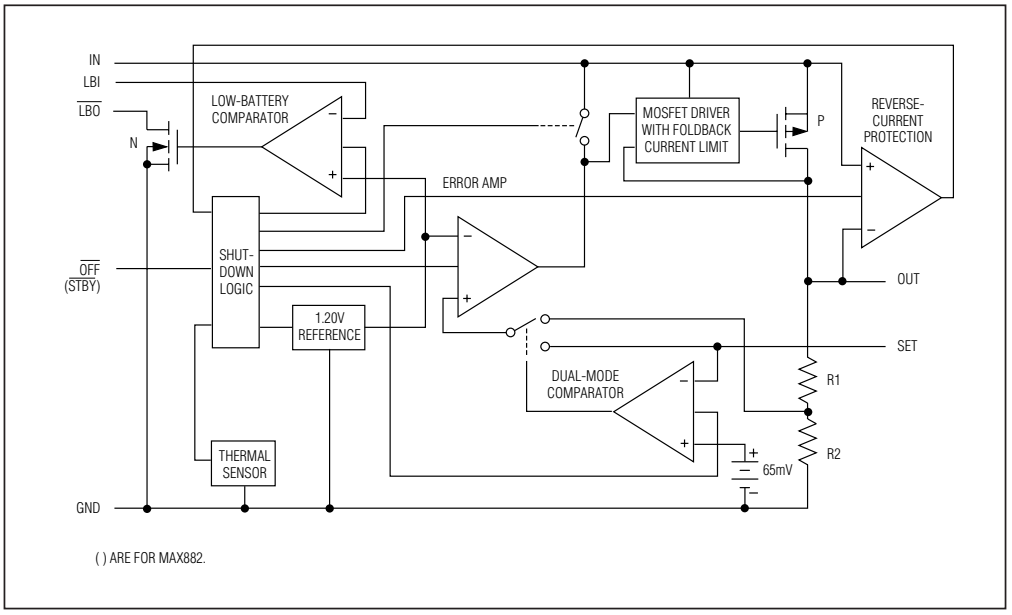


Figure 1. MAX882/MAX883/MAX884 Functional Diagram

In adjustable mode, the user selects an output voltage in the 1.25V to 11V range by connecting two external resistors, used as a voltage-divider, to the SET pin (Figure 2).

The output voltage is set by the following equation:

$$V_{OUT} = V_{SET}\left(1 + \frac{R1}{R2}\right)$$

where V_{SET} = 1.20V.

To simplify resistor selection:

$$R1 = R2\left(\frac{V_{OUT}}{V_{SET}} - 1\right)$$

Since the input bias current at SET is nominally zero, large resistance values can be used for R1 and R2 to minimize power consumption without losing accuracy. Up to 1.5MΩ is acceptable for R2. Since the V_{SET} tolerance is less than ±40mV, the output can be set using fixed resistors instead of trim pots.

Standby Mode (MAX882)

The MAX882 has a standby feature that disconnects the input from the output when STBY is brought low, but keeps all other circuitry awake. In this mode, V_{OUT} drops to 0, and the internal biasing circuitry (including the low-battery comparator) remains on. The maximum quiescent current during standby is 15µA. STBY is a comparator input with the other input internally tied to the reference voltage. Use a resistor network as shown in Figure 3 to set a standby-mode threshold voltage for undervoltage lockout. Connect STBY to IN for normal operation.

OFF Mode (MAX883/MAX884)

A low-logic input on the OFF pin shuts down the MAX883/MAX884. In this mode, the pass transistor, control circuit, reference, and all biases are turned off, and the supply current is reduced to less than 1µA. $\overline{LBO}$ is undefined in OFF mode. Connect OFF to IN for normal operation.

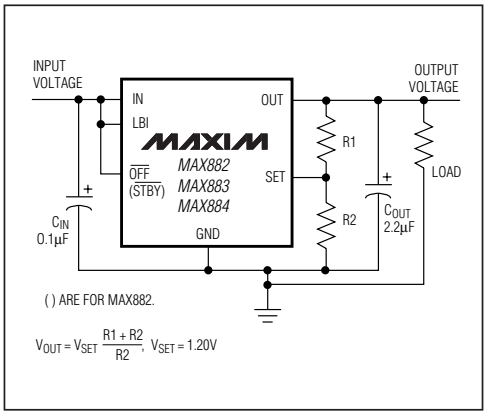


Figure 2. Adjustable Output Using External Feedback Resistors

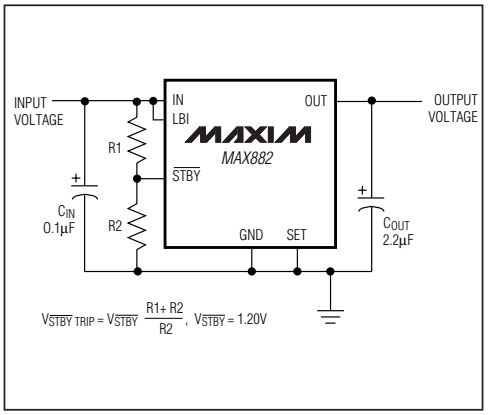


Figure 3. Setting an Undervoltage Lockout Threshold Using STBY

Foldback Current Limiting

The MAX882/MAX883/MAX884 also include a foldback current limiter. It monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to 430mA for output voltages above 0.8V and (V_{IN} - V_{OUT}) > 0.7V. If the output voltage drops below 0.8V, implying a short-circuit condition, the output current is limited to 170mA. The output can be shorted to ground for 1min without damaging the device if the package can dissipate (V_{IN} x 170mA) without exceeding T_J = +150°C. When the output is greater than 0.8V and (V_{IN} - V_{OUT}) < 0.7V (dropout operation), no current limiting is allowed, to provide maximum load drive.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX882/MAX883/MAX884. When the junction temperature exceeds T_J = +160°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by 10°C, resulting in a pulsed output during thermal overload conditions.

Thermal overload protection is designed to protect the MAX882/MAX883/MAX884 if fault conditions occur. It is not intended to be used as an operating mode. Prolonged operation in thermal-shutdown mode may reduce the IC's reliability. For continual operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Power Dissipation and Operating Region

Maximum power dissipation of the MAX882/MAX883/MAX884 depends on the thermal resistance of the case and PC board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The resulting power dissipation is as follows:

$$P = \frac{(T_J - T_A)}{(\theta_{JB} + \theta_{BA})}$$

where (T_J - T_A) is the temperature difference between the MAX882/MAX883/MAX884 die junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package chosen, and θ_{BA} is the thermal resistance through the PC board, copper traces, and other materials to the surrounding air.

The 8-pin small-outline package for the MAX882/MAX883/MAX884 features a special lead frame with a lower thermal resistance and higher allowable power dissipation. This package's thermal resistance package is θ_{JB} = 53°C/W, compared with θ_{JB} = 110°C/W for an 8-pin plastic DIP package and θ_{JB} = 125°C/W for an 8-pin ceramic DIP package.

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

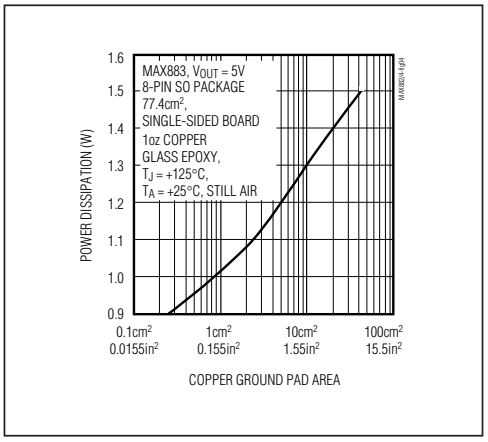


Figure 4. Typical Maximum Power Dissipation vs. Ground Pad Area

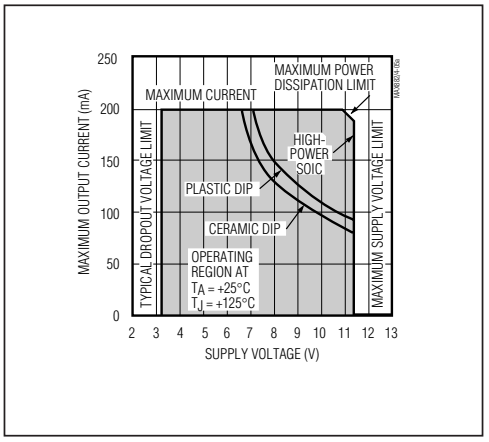


Figure 5a. Safe Operating Regions: MAX882/MAX884 Maximum Output Current vs. Supply Voltage

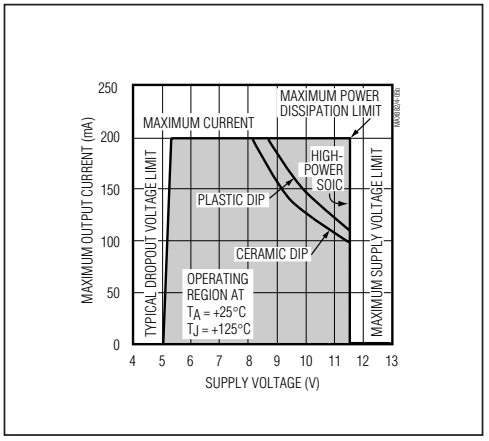


Figure 5b. Safe Operating Regions: MAX883 Maximum Output Current vs. Supply Voltage

The GND pins of the MAX882/MAX883/MAX884 SOIC package perform the dual function of providing an electrical connection to ground and channeling heat away. Connect all GND pins to ground using a large pad or ground plane. Where this is impossible, place a copper plane on an adjacent layer. For a given power dissipation, the pad should exceed the associated dimensions in Figure 4.

Figure 4 assumes the IC is in an 8-pin small-outline package that has a maximum junction temperature of +125°C and is soldered directly to the pad; it also has a +25°C ambient air temperature and no other heat sources. Use larger pad sizes for other packages, lower junction temperatures, higher ambient temperatures, or conditions where the IC is not soldered directly to the heat-sinking ground pad. When operating C- and E-grade parts up to a T_J of +125°C, expect performance similar to M-grade specifications. For T_J between +125°C and +150°C, the output voltage may drift more.

The MAX882/MAX883/MAX884 can regulate currents up to 250mA and operate with input voltages up to 11.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltages are small, as shown in Figure 5. Maximum power dissipation depends on packaging, temperature, and air flow. The maximum output current is as follows:

$$I_{OUT(MAX)} = \frac{P(T_J - T_A)}{(V_{IN} - V_{OUT})100°C}$$

where P is derived from Figure 4.

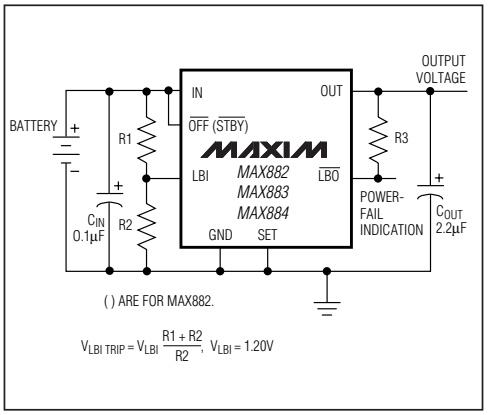


Figure 6. Using the Low-Battery Comparator to Monitor Battery Voltage

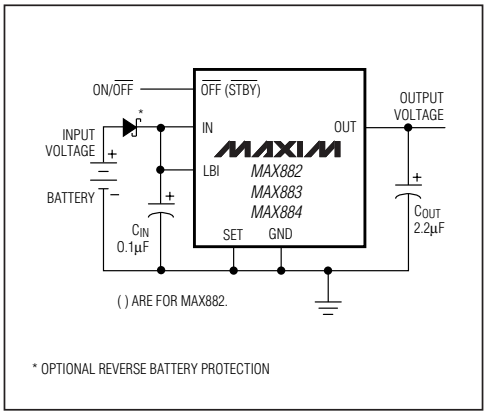


Figure 7. Typical 3.3V or 5V Linear Regulator Circuit

Reverse-Current Protection

The MAX882/MAX883/MAX884 have a unique protection scheme that limits reverse currents when the input voltage falls below the output. It monitors the voltages on IN and OUT and switches the IC's substrate and power bus to the more positive of the two. The control circuitry is then able to remain functioning and turn the pass transistor off, limiting reverse currents back through to the input of the device. In this mode, typical current into OUT to GND is 15µA at V_{OUT} = 3.3V and 50µA at V_{OUT} = 5V.

Reverse-current protection activates when the voltage on IN falls 6mV (or 20mV max) below the voltage on OUT. Before this happens, currents as high as several milliamperes can flow back through the device.

Low-Battery-Detection Comparator

The MAX882/MAX883/MAX884 provide a low-battery comparator that compares the voltage on the LBI pin to the 1.20V internal reference. $\overline{LBO}$, an open-drain output, goes low when LBI is below 1.20V. Hysteresis of 7mV has been added to the low-battery comparator to provide noise immunity during switching. $\overline{LBO}$ remains functional in standby mode for the MAX882, but is undefined in OFF mode for the MAX883 and MAX884. Tie LBI to IN when not used.

Use a resistor-divider network as shown in Figure 6 to set the low-battery trip voltage. Current into the LBI input is ±50nA (max), so R2 can be as large as 1MΩ. Add extra noise immunity by connecting a small capacitor from LBI to GND. Additional hysteresis can be added by connecting a high-value resistor from LBI to $\overline{LBO}$.

Applications Information

The MAX882/MAX883/MAX884 are series linear regulators designed primarily for battery-powered systems. Figure 7 shows a typical application.

Standby Mode vs. OFF Mode

STBY is a comparator input that allows the user to set the standby-mode threshold voltage, while OFF is a logic-level input. When in standby mode, the output is disconnected from the input, but the biasing circuitry (including the low-battery comparator) is kept alive, causing the device to draw approximately 7µA. Standby mode is useful in applications where a low-battery comparator function is still needed in shutdown.

A logic low at the $\overline{OFF}$ pin turns off all biasing circuitry, including the LBI/$\overline{LBO}$ comparator, and reduces supply current to less than 1µA. OFF mode is useful for maximizing battery life. There is little difference in the time it takes to exit standby mode or OFF mode.

Output Capacitor Selection and Regulator Stability

An output filter capacitor is required at the MAX882/MAX883/MAX884 OUT pin. The minimum output capacitance required for stability is 2.2µF.

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

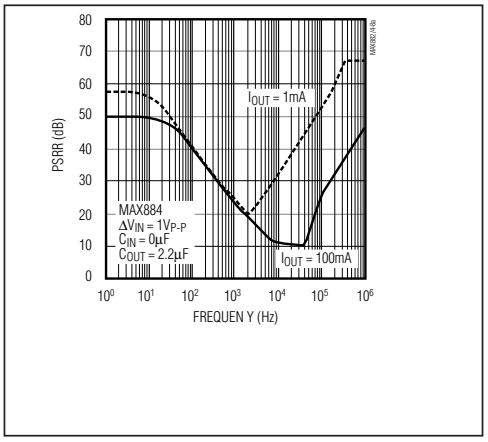


Figure 8a. Power-Supply Rejection Ratio vs. Ripple Frequency for Light and Heavy Loads

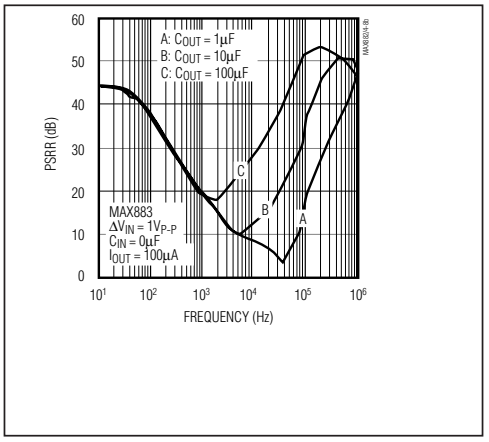


Figure 8b. Power-Supply Rejection Ratio vs. Ripple Frequency for Various Output Capacitances

The filter capacitor's size depends primarily on the desired power-up time and load-transient responses. Load-transient response is improved by using larger output capacitors.

The output capacitor's equivalent series resistance (ESR) will not affect stability as long as the minimum capacitance requirement is observed. The type of capacitor selected is not critical, but it must remain above the minimum value over the full operating temperature range.

Input Bypass Capacitor

Normally, use 0.1µF to 10µF capacitors on the MAX882/MAX883/MAX884 input. The best value depends primarily on the power-up slew rate of V_{IN}, and on load and line transients. Larger input capacitor values provide better supply-noise rejection and line-transient response, as well as improved performance, when the supply has a high AC impedance. The type of input bypass capacitor used is not critical.

Noise

The MAX882/MAX883/MAX884 exhibit up to 4mV_{p-p} of noise during normal operation. This is negligible in most applications. When using the MAX882/MAX883/MAX884 for applications that include analog-to-digital converters (ADCs) with resolutions greater than 12 bits, consider the ADC's power-supply rejection specifications. See the output noise plot in the *Typical Operating Characteristics* section.

PSRR and Operation from Sources Other than Batteries

The MAX882/MAX883/MAX884 are designed to achieve low dropout voltages and low quiescent currents in battery-powered systems. However, to gain these benefits, the devices must trade away power-supply noise rejection, as well as swift response to supply variations and load transients. For a 1mA load current, power-supply rejection ranges from 60dB down to 20dB at 2kHz. At higher frequencies, the circuit depends primarily on the characteristics of the output capacitor, and the PSRR increases (Figure 8).

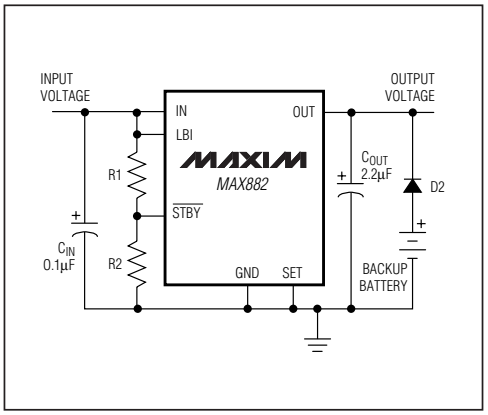


Figure 9. Short-Term Battery Backup Using the MAX882

When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the values of the input and output capacitors and employing passive filtering techniques. Do not use power supplies with ripple voltage exceeding 200mV at 100kHz.

Overshoot and Transient Considerations

The *Typical Operating Characteristics* section shows power-up, supply, and load-transient response graphs. On the load-transient graphs, two components of the output response can be observed: a DC shift from the output impedance due to the different load currents, and the transient response. Typical transients for step changes in the load current from 50mA to 250mA are 200mV. Increasing the output capacitor's value attenuates transient spikes.

During recovery from shutdown, overshoot is negligible if the output voltage has been given time to decay adequately. During power-up from V_{IN} = 0, overshoot is typically less than 1% of V_{OUT}.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX882/MAX883/MAX884 use a p-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*). Quickly stepping up the input voltage from the dropout voltage can result in overshoot.

Short-Term Battery Backup Using the MAX882

Figure 9 illustrates a scheme for implementing battery backup for 3.3V circuits using the MAX882. When the supply voltage drops below some user-specified value based on resistors R1 and R2, the standby function activates, turning off the MAX882's output. Under these conditions, the backup battery supplies power to the load. Reverse current protection prevents the battery from draining back through the regulator to the input.

This application is limited to short-term battery backup for 3.3V circuits. The current drawn by the MAX882's OUT pin at 3.3V during reverse-current protection is typically 8µA. It should not be used with the MAX883 and MAX884, since the OFF pin is a logic input, and indeterminate inputs can cause the regulator to turn on intermittently, draining the battery.

Reverse Battery Protection

Reverse battery protection can be added by including an inexpensive Schottky diode between the battery input and the regulator circuit, as shown in Figure 7. However, the dropout voltage of the regulator will be increased by the forward voltage drop of the diode. For example, the forward voltage of a standard 1N5817 Schottky diode is typically 0.29V at 200mA.

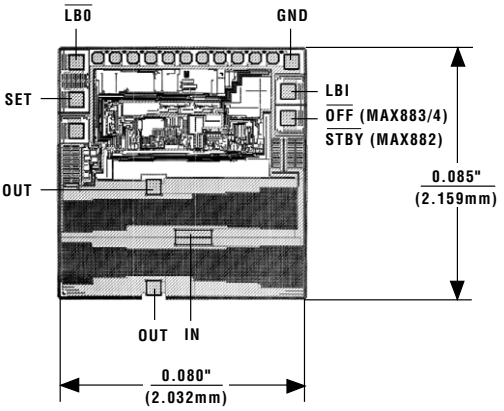
5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX883CPA	0°C to +70°C	8 PDIP
MAX883CSA	0°C to +70°C	8 SO
MAX883C/D	0°C to +70°C	Dice*
MAX883EPA	-40°C to +85°C	8 PDIP
MAX883ESA	-40°C to +85°C	8 SO
MAX883MPA/PR	-55°C to +125°C	8 PDIP
MAX884CPA	0°C to +70°C	8 PDIP
MAX884CSA	0°C to +70°C	8 SO
MAX884C/D	0°C to +70°C	Dice*
MAX884EPA	-40°C to +85°C	8 PDIP
MAX884ESA	-40°C to +85°C	8 SO

*Dice are tested at T_J = +25°C, DC parameters only.
**Contact factory for availability.

Chip Topography

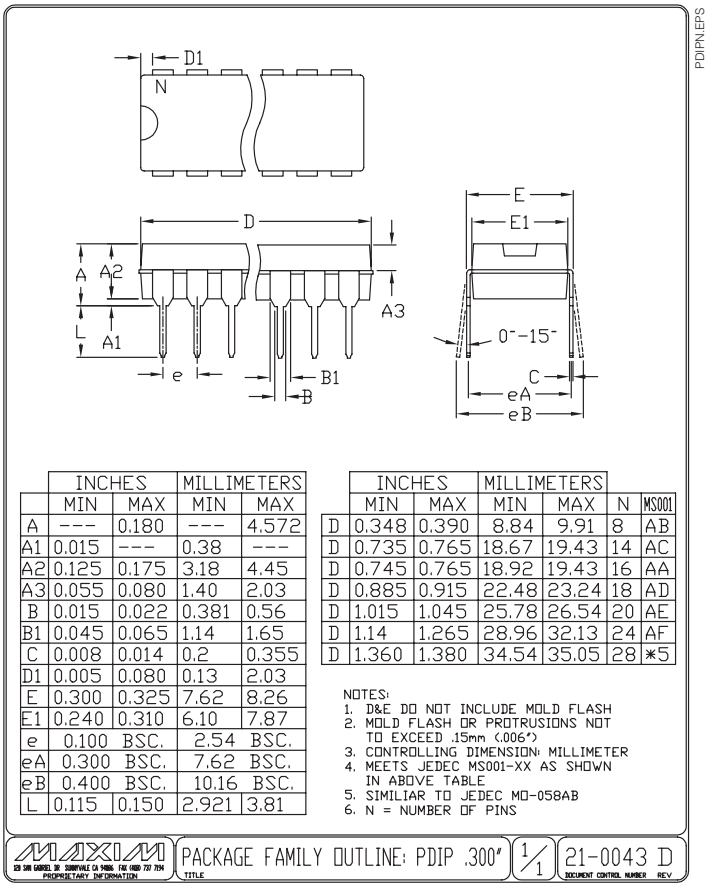


NO DIRECT SUBSTRATE CONNECTION. THE N-SUBSTRATE IS INTERNALLY SWITCHED BETWEEN THE MORE POSITIVE OF IN OR OUT.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8-T	21-0043
8 SO	S8-6F	21-0041



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300" TITLE

1/1

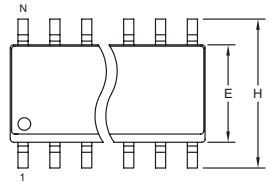
21-0043 D DOCUMENT CONTROL NUMBER REV

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

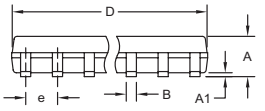
Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

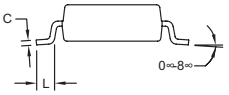
SOICN .EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	9/08	Added information for rugged plastic product.	14
4	7/09	Revised *Ordering Information* table.	14