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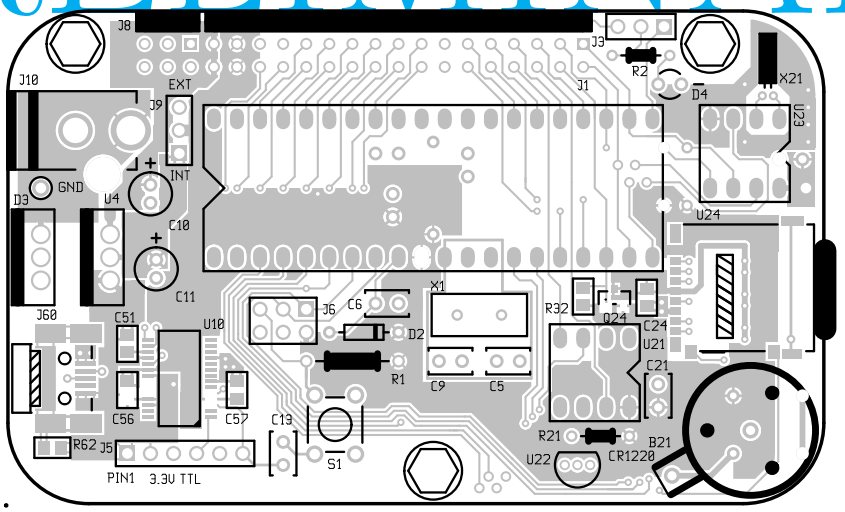

NB2AS Description

The NB2AS is a microcontroller development system that is compatible with the Arduino/Sanguino software environment. For system development a variety of peripherals are available.

Features

- Replaceable and upgradeable CPU
- Compatible with the Arduino/Sanguino development tools.
- ATmega644P running at 12MHz with a V_{CC} of 3.3V.
- SMD land patterns designed for hand assembly.
- 3.55" x 2.15" (Fits in the larger Altoids tin)
- Atmega I/O connections, DAC outputs and RTC interrupt output lines are wired to a single 34 pin header. Application boards can be mounted parallel using vertical connectors, co-planar using right-angle connectors or remotely using a cable.
- microSD Card
  - Series MOSFET enables power to be cycled on the uSD card. This enables the uSD to be properly reset.
  - Card-detect output wired to an I/O line.
  - Tested with Transcend 1GB, Sandisk 2GB and Sandisk 4GB HC.
- DAC Features
  - Two channels, twelve bits per channel, SPI interface.
  - Reference – 1.225V, ±0.1% (initial accuracy), 100ppm per °C maximum drift,
- RTC Features
  - Real-Time Clock (RTC) counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100
  - Two Time-of-Day Alarms
  - Programmable Square-Wave Output
  - Backup power from a CR1220 coin cell.
  - I^2C Serial Interface
- The board can be built with either a USB interface or with a six pin header for use with an USB to serial cable. The USB interface circuitry includes transient suppression.
- ICSP port (3.3V levels)
- A/D reference supply filtered per Atmel specification.
- Reset circuit per Atmel specification.
- Power supply is jumpered between either an LDO or an external 3.3V supply. The LDO input is diode or'ed from a wall adapter or the USB 5V supply.
- The NB2AS accessories include an Li-ion charger, prototyping board and a terminal block interface.

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1 Assembling the NB2AS

Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

The Bill of Materials (BOM) and Component List are in section 7. For full page assembly drawings see Figure 1 (top) and Figure 2 (bottom).

Extra care needs to be taken when soldering the right-angle connector(s) – `J1` and `J8` (opt). The outer edge of the connector bodies should not protrude over the edge of the board. After soldering and the connector pins should be parallel to the board.

A DC source with current limiting is useful for testing each section of the NB2AS as you build it.

All of the headers supplied with the kit are breakaway headers. The single row headers, `J3` (3x1), `J5` (6x1), `J9` (3x1) may come as individual headers or as strips that need to be broken. Most kits will contain either two 6x1 headers or one 12x1. Break these headers to create `J3`, `J5` and `J9`.

If you are not building the USB circuit proceed to subsection 1.4.

1.1 microSD Circuit Assembly (Top)

Solder the top side components:

- U24 (uSD socket)
- Q24
- C24
- R32

1.2 USB Circuit Assembly (Top)

Solder the top side components:

- J60
- U10 - FT232RL
- C57, C56, C51
- R62

1.3 SMD Components (Bottom)

Solder the bottom side components:

- R25, R27, R28
- R24
- R26
- U55
- R59
- R58
- F1

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints.

1.4 Bottom Side Components

- C1, C2, C3
- L1

  The value of inductor L1 is not critical. Kits will contain an inductor with a value between 10µH and 15µH
- D21, D22
- C23

1.5 Power Supply Circuit Assembly

Solder the top side components:

- C10, C11

  C10 and C11 are polarized parts. The long lead is the positive. The short lead is the negative. Make sure that the **positive** *lead is inserted into positive hole in the PCB*
- U4

  Be careful to not mixup U4 and D3. U4 is marked `MC33269T-3.3G` *Make sure that the tab is aligned to the tab marking on the PCB.*
- D3

  Be careful to not mixup D3 and U4. D3 is marked `MBR1545CTG` *Make sure that the tab is aligned to the tab marking on the PCB.*
- J9
- J10
- J8 (optional)

  J8 enables the usage of an external 3.3V power source with the NB2AS. If you do not need this function then you can omit the installation of J8. J8 is not included in the kit.

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints.

1.5.1 Testing the Power Supply Circuit

If possible apply power through `J10` with a current limited +5V supply. The current drawn from the +5V supply should not exceed a few milliamperes. If it does then verify the orientation on `C10`, `C11`, `D3`, `U4`.

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1.6 Microcontroller Circuit Assembly

Solder the top side components:

- R1

  The tolerance of R1 is not critical. The 1% resistor has five color bands (brown, black, black, red, brown)

- D2

  Line the cathode marking on D1 with the cathode marking on the silkscreen

- C13, C6 (optional).

  C6 is optional and is not included in the kit. It is meant for applications that require additional filtering of the reset line. Applications that use USB download or ISP programmers like the AVRISPMKII will not require additional filtering. Also, the reset function that uses the /RTS line from the USB interface will not function with C6 installed.

- D4

  The negative lead of the LED is the short lead. Align the short lead with the negative marking on the PCB.

- R2

  The tolerance of R2 is not critical. The 1% resistor has five color bands (red, red, brown, black, brown).

- J3
- X1, C5, C9
- U1 (socket)
- J6
- J1

  J1 that is included with the NB2AS Kit are right angle connectors. If your application requires parallel board mounting or a cable connection then replace J1 with vertical headers. A 2x17 receptacle can also be used.

- J4 (optional).

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints. After inserting an ATmega644P into the `U1` socket the microcontroller section of the NB2AS should be fully functional. If possibly apply power through `J10` with a current limited +5V supply. The current drawn should not exceed 10mA (20mA if the `J3` jumper is installed in the VCC position).

1.7 RTC Circuit Assembly

`R22` and `R23` are the I^2C pullups. The value included in the NB2A kit is 4.7KΩ. If you are running the I^2C bus at lower frequencies you could increase the value of these resistors. If your application has external pullups you should remove these resistors (See subsection 5.1).

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Sanguion pin ??) and PD5 (Sanguino pin ??) respectively. To disconnect `/INTA` cut jumper J24. To disconnect `/INTB` cut jumper J25 (See subsection 5.2).

- R22, R23

  The tolerance of R22 and R23 is not critical. Some kits include a 5% resistor others include a 1% resistor. The 5% resistor has four color bands (yellow, violet, red, gold). The 1% resistor has five color bands (yellow, violet, black, brown, brown).

- B21 battery holder
- X21 crystal

  If you are assembling a revision one PCB then see **??**.

- U23 socket

1.8 DAC Circuit Assembly

- R21
- U22
- C21
- U21 socket

1.9 Electro-mechanical Components

The electro-mechanical components are sensitive to washing. Place all of these last and lightly wash afterward. If water does get into these components let them dry out before applying power.
Solder the top side components:

- S1

1.10 Mounting Hardware

Space has been provided for three #2 hex standoffs and washers.

1.11 IC Installation and Test

Remove each IC from the antistatic foam and insert it into the appropriate socket aligning the notch in the IC package with notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

- ATmega644P (`U1`)
- TLV5618 (`U21`)
- DS1337 (`U32`)

The board is now ready to program. To test the programming using the Arduino/Sanguino tools (see **??**).

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2 IO Connectors

J1	17x2 header	I/O connections from the ATmega644P. See Table 2
J3	3x1 header	Jumper to switch the debug LED between 3.3V (right position) and ATmega644P pin PD7 (left position) (Sanguino pin 15)
J5	6x1 header	USB header for an FTDI TTL-232R-3V3 cable. This is only installed if the USB circuit is not populated.
J6	3x2 header	ICSP header
J8	3x2 header	External 3.3V regulated voltage input. See Table 3
J9	3x1 jumper	Jumper to switch between the external 3.3V input and the on board LDO.
J10	2.1mm Jack	5V to 15V unregulated DC. The power dissipation in U4 needs to be kept below one watt.
J60	USB Mini-B	

Table 1: NB2AS connectors

2.1 J1 Header

NB2AS		ATmega644P		Sanguino
Pin	**Function**	**Pin**	**Function**	**Pin**
1	PC0/SCL	22	PC0/SCL	D16
2	PD5	19	PD5	D13
3	PC1/SDA	23	PC1/SDA	D17
4	PD4	18	PD4	D12
5	PC2	24	PC2	D18
6	DACB			
7	PC3	25	PC3	D19
8	DACA			
9	PC4	26	PC4	D20
10	PD3/TXD1	17	PD3/TXD1	D11
11	PC5	27	PC5	D21
12	PD2/RXD1	16	PD2/RXD1	D10
13	GND	31	GND	
14	GND	31	GND	
15	PA7/ADC7	33	PA7/ADC7	A7/D24
16	PB7/SCK	8	PB7/SCK	D7
17	PA6/ADC6	34	PA6/ADC6	A6/D25
18	PB6/MISO	7	PB6/MISO	D6
19	PA5/ADC5	35	PA5/ADC5	A5/D26
20	PB5/MOSI	6	PB5/MOSI	D5
21	PA4/ADC4	36	PA4/ADC4	A4/D27
22	PB4	5	PB4	D4
23	PA3/ADC3	37	PA3/ADC3	A3/D28
24	PB3	4	PB3	D3
25	PA2/ADC2	38	PA2/ADC2	A2/D29
26	PB2	3	PB2	D2
27	PA1/ADC1	39	PA1/ADC1	A1/D30
28	PB1	2	PB1	D1
29	PA0/ADC0	40	PA0/ADC0	A0/D31
30	PB0	1	PB0	D0
31	3.3V			
32	3.3V			
33	VBUS			
34	VBUS			

Table 2: J1 Pinout

2.2 J8 Header

Pin	Function
1	3.3V EXT
2	3.3V EXT
3	GND
4	GND
5	BSTAT
6	NC

Table 3: J8 Pinout

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3 Electrical Hints

3.1 Power Supply

The NB2AS can be powered by a wall adapter, the USB port or an external regulated 3.3V supply. The wall adapter and the USB port are diode or'ed and are connected to the input of a LDO regulator (U4). Jumper J9 selects between the two power sources – INT is the LDO regulator (U4), EXT is the power source connected to J8.

Power Jumper in the Internal Position

Power Jumper in the External Position

It is critcal to keep the power dissipation in the LDO regulator (U4), to less than one watt. The voltage drop across U4 is

$$V_{drop} = V_{in} - 0.5V - 3.3\text{V}$$

where V_{in} is the greater of the wall adapter voltage or $+5V$ (USB 5V supply). The power dissipated in U4 is given by

$$P_{diss} = V_{drop} \cdot I_{system}$$

where I_{system} is the load of the NB2AS plus its peripheral circuitry.

3.2 Powering from the USB Port

The intial startup load of a device connected to the USB port must not exceed 10μF in parallel with 44Ω (USB-IF, 2000a). Peripheral circuitry attached to the NB2AS may produce a system load that exceeds the specification.

3.3 V_{BUS}

V_{BUS} is the unregulated voltage at the cathode of the or'ing diode (D3). Applications that require current beyond the current rating of the LDO regulator (U4) should use V_{BUS}. Since the only volage drop between the input power source and V_{BUS} is the V_F of the or'ing diode (D3) it is more efficient to use V_{BUS} rather than the +3.3V supply as an input voltage for other power conversions.

3.4 Debug LED

The debug LED, `D4`, can be connected to the +3.3V supply or to `U1` pin 21 (PD7) of the ATmega644P. `U1` pin 21 corresponds to Sanguino pin "15".

LED jumper in the VCC position

LED jumper in the PD7 position

4 Programming the NB2AS

The NB2AS can be programmed using the Arduino tools (version `0011` or more recent) with the Sanguino extensions (See Sanguino Hints) using the USB interface from a PC or MAC. If you purchased a board with a USB interface than connect a USB Mini-B cable to J60. If you purchased a board with an FTDI header then connect the FTDI receptacle to J5 matching pin one of the cable to the pin one marking on the board.

4.1 Selecting the proper board

In order for the Arduino tools to recoginze a new board the `boards.txt` file needs to be modified. As part of the Sanguino tools installation the Sanguino parameters where added to the `boards.txt` file.

An easy way to add entries for the NB2AS is to copy the Sanguino entries and make the following changes to the copied lines –

1. Change all occurances of `Sanguino` to `nb2as`
2. Change the `name` to `NB2AS` (Line 1)
3. Change the `maximum_size` to `61440` (Line 3)
4. Change the `f_cpu` to `12000000L` (Line 13)
5. Change the `core` to `nb2as` (Line 14)
6. Change the `high_fuses` to `0xDA` (Line 6)

The modified lines are shown in Listing 1 (with annotations).

Listing 1: Modifications to the boards.txt file for the NB2AS

```
1 nb2as.name=NB2AS
2 nb2as.upload.protocol=stk500
3 nb2as.upload.maximum_size=61440
4 nb2as.upload.speed=38400
```

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```
nb2as.bootloader.low_fuses=0xFF
nb2as.bootloader.high_fuses=0xDA
nb2as.bootloader.extended_fuses=0xFD
nb2as.bootloader.path=atmega644p
nb2as.bootloader.file=ATmegaBOOT_644P.hex
nb2as.bootloader.unlock_bits=0x3F
nb2as.bootloader.lock_bits=0x0F
nb2as.build.mcu=atmega644p
nb2as.build.f_cpu=12000000L
nb2as.build.core=nb2as
nb2as.verbose=false
```

With a modified `boards.txt` select `nb2as` from the `Tools->Board` menu.

4.2 Downloading a program to the NB2AS

The NB2AS must be rebooted to start program download. This can be done by pressing the reset button `S1` immediately before starting the download. If your USB port is configured to `set RTS on close` then the reset will occur automatically.

4.3 Downloading a bootloader

The NB2AS is powered from 3.3V. Any device that connects to the NB2AS needs to output 3.3V TTL levels. The Atmel `AVRATAVRISPMKII` and Ladyada USBtiny are compatible with the NB2AS.

To use the Ladyada USBtiny remove the USBtiny jumper, JP3, and plug the USBtiny cable into the NB2AS ICSP header. With JP3 removed the USBtiny output buffer (IC2) is powered by the V_{cc} from the NB2AS (3.3V). The USBtiny output buffer (IC2) is a `74AHC125` which will tolerate 5V levels when powered from a 3.3V supply.

5 Real-Time Clock

The NB2AS real-time clock (RTC) consists of a DS1337 that is powered by a CR1220 coin cell. Communication to the DS1337 is through the I^{2}C interface (a.k.a. two-wire or TWI). The I^{2}C pullup resistors on the NB2AS are 4.7KΩ. The interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Sanguino pin 6) and PD5 (Sanguino pin 5) respectively. There are no pullup resistors on the interrupt lines. If external pullups are not added then the internal pullups of the ATmega644P need to be used.

Programming the RTC requires a software library for the DS1337 and for the TWI interface. Both of these libraries are available for download at wiblocks.

5.1 I^{2}C Pullup Resistors

The maximum bus capacitance of the I^{2}C bus is 400pF. Unless a large number of devices are on the bus or devices are connected using long cables an NB2AS system will not get close to this limit. The DS1337 represents a maximum load of 10pF.

The mimunum pullup resistance is 966Ω ($\frac{V_{CC}-0.4V}{3mA}$). The maximum value pullup resistance is

$$R_{pullup(max)} = \begin{cases} \frac{1000nS}{C_{BUS}} & \text{if } F_{SCL} \leq 100kHz, \\ \frac{300nS}{C_{BUS}} & \text{if } 100kHz < F_{SCL} \leq 400kHz. \end{cases}$$

where C_{BUS} is the maximum bus capacitance, , and V_{CC} is 3.3V for the NB2AS.

With a 100pF load (10 times the DS1337 load), the maximum resistance for 400kHz operation is 3KΩ. For 100kHz the maximum resistance is 10KΩ. If only the DS1337 is on the I^{2}C bus the maximum resistances would be 100KΩ (100kHz) and 30KΩ (400kHz). The minimum resistance, which is not dependent on bus capacitance, is 966Ω for any operating frequency and C_{BUS}. (Atmel, 2009a)

5.2 DS1337 Interrupt Lines

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Sanguino pin 6) and PD5 (Sanguino pin 5) respectively. To disconnect `/INTA` cut jumper `J24`. To disconnect `/INTB` cut jumper `J25`.

There are no pullup resistors connected to the interrupt lines. To use the interrupt lines with the ATmega644P the internal pull-up resistors need to be enabled. For the ATmega644P 20KΩ $\leq R_{pullup} \leq$ 50KΩ which is sufficient to pullup the DS1337 lines. (Atmel, 2009b).

5.3 RTC Battery Life

The DS1337 operates with a V_{CC} from 1.8V to 5.5V. On the NB2AS the V_{CC} line is diode or'ed between the CR1220 coin cell and the 3.3V supply. The capacity of the CR1220 is 40mAH (to 2V). When the I2C bus is active the DS1337 is supplied from the 3.3V supply. When the device is inactive the DS1337 is in standby mode which has a maximum current is 1.5μA.(Maxim, 2009a) The maximum battery life is ≈ 26000 hours.

6 Dual DAC

The dual DAC on the NB2AS is the Texas Instruments TLV5618 which has a resolution of 12 bits. Communication to the DAC is through the SPI interface. Data is shifted into the shift register. After 16bits of data is shifted or the `/CS` line rises the contents of the shift register is transferred to the target latches. The selection of the target latches is set by the control bits.

The reference used is the LM4041. The reference voltage is 1.225V, ±0.1% (initial accuracy), 100ppm per °C maximum drift. Since the NB2AS is a 3.3V system the maximum reference voltage for the TLV5618 is 1.8V.

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7 Assembly Documentation and Schematics

Table 4: Bill of Materials

Kit: NB2AS-KIT3

Qty	Reference	Part Number	Description
1	B21	CON_BAT__Keystone_500	connector, battery, CR1220
7	C1, C2, C3, C6, C13, C21, C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
2	C5, C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
2	C10, C11	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
4	C24, C51, C56, C57	CAPC-0U1-50V-X7R-0805	capacitor, ceramic, 0.1uF, 16V, 0805
1	D2	DIOA-1N4148	diode, 1N4148
1	D3	DIO__On-Semi_MBR1545CTG	diode, dual, On-Semi MBR1545CTG
1	D4	LEDR-1T-GRN-2M00	LED, T1, Green
2	D21, D22	DIOA-BAT41	diode, BAT41
1	F1	FUSE__Littelfuse_1812L050PR	fuse, 0.5A 1812
1	J1	HDR_RA_BR-17X2-100M	header, RA, 17x2, 100mils
2	J3, J9	HDR_BR-3X1-100M	header, 3x1, 100mils
1	J6	HDR_BR-3X2-100M	header, 3x2, 100mils
1	J10	CON__CUI-PJ-202AH	power jack, 2.1mm
1	J60	Molex_67503-1020	
1	L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
1	Q24	FET_P__On-Semi_NTR4101PT1G	FET, P, -20V, 3.2A
1	R1	RES-10K0-0W25-1T00	resistor, 10K, 1/4W, 1%
1	R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
1	R21	RES-2K10-0W125-1T00	resistor, 2.1K, 1/8W, 1%
2	R22, R23	RES-4K70-0W125-1T00	resistor, 4.7K, 1/8W, 1%
3	R24, R58, R62	RES-10K0-0805-1T00	resistor, 10K, 0805. 1%
3	R25, R27, R28	RESCAV-47K0-0W125-5T00-2N	resistor network, 47K, 1/8W, 1206x2 Concave
2	R26, R32	RES-47K5-0805-1T00	resistor, 47.5K, 0805, 1%
1	R59	RES-4K70-0805-1T00	resistor, 4.7K, 0805, 1%
1	S1	SW__Panasonic_EVQ-PAE04M	pushbutton
1	U1	IC__ATMEL_ATmega644P-20PU	ATmega644P-20PU, 64K/4K/2K, 20MHz
1	U4	VREG__On-Semi_MC33269T-3.3G	voltage regulator, 3.3V, 800mA, TO-220
1	U10	FTDI_FT232RL	
1	U21	IC_DAC__TI_TLV5618	IC, DAC, TLV5618, 2ch, 12bit, DIP-8
1	U22	IC_REF__LM4041AIZ-1.2	IC, REF, 1.225V, 0.1%, TO-92
1	U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1377+
1	U24	Molex_502702-0891	
1	U55	TI_SN65220DBV	
1	X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
1	X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
2		DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
1		DIP-40P-600M	DIP Socket, 40 Pin, 600mil centers
2		JMP__Adamtech_MSBHG	Shunt with handle
1		BAT-CR1220	battery, coin cell, CR1220
1		wiblock_NB2AS-PCB	

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Table 5: Component List

Kit: NB2AS-KIT3

Reference	Part Number	Description
B21	CON_BAT__Keystone_500	connector, battery, CR1220
C1	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C6	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C13	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C21	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C5	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C10	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C11	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C24	CAPC-0U1-50V-X7R-0805	capacitor, ceramic, 0.1uF, 16V, 0805
C51	CAPC-0U1-50V-X7R-0805	capacitor, ceramic, 0.1uF, 16V, 0805
C56	CAPC-0U1-50V-X7R-0805	capacitor, ceramic, 0.1uF, 16V, 0805
C57	CAPC-0U1-50V-X7R-0805	capacitor, ceramic, 0.1uF, 16V, 0805
D2	DIOA-1N4148	diode, 1N4148
D3	DIO__On-Semi_MBR1545CTG	diode, dual, On-Semi MBR1545CTG
D4	LEDR-1T-GRN-2M00	LED, T1, Green
D21	DIOA-BAT41	diode, BAT41
D22	DIOA-BAT41	diode, BAT41
F1	FUSE__Littelfuse_1812L050PR	fuse, 0.5A 1812
J1	HDR_RA_BR-17X2-100M	header, RA, 17x2, 100mils
J3	HDR_BR-3X1-100M	header, 3x1, 100mils
J9	HDR_BR-3X1-100M	header, 3x1, 100mils
J6	HDR_BR-3X2-100M	header, 3x2, 100mils
J10	CON__CUI-PJ-202AH	power jack, 2.1mm
J60	Molex_67503-1020	
L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
Q24	FET_P__On-Semi_NTR4101PT1G	FET, P, -20V, 3.2A
R1	RES-10K0-0W25-1T00	resistor, 10K, 1/4W, 1%
R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
R21	RES-2K10-0W125-1T00	resistor, 2.1K, 1/8W, 1%
R22	RES-4K70-0W125-1T00	resistor, 4.7K, 1/8W, 1%
R23	RES-4K70-0W125-1T00	resistor, 4.7K, 1/8W, 1%
R24	RES-10K0-0805-1T00	resistor, 10K, 0805. 1%
R58	RES-10K0-0805-1T00	resistor, 10K, 0805. 1%
R62	RES-10K0-0805-1T00	resistor, 10K, 0805. 1%
R25	RESCAV-47K0-0W125-5T00-2N	resistor network, 47K, 1/8W, 1206x2 Concave
R27	RESCAV-47K0-0W125-5T00-2N	resistor network, 47K, 1/8W, 1206x2 Concave
R28	RESCAV-47K0-0W125-5T00-2N	resistor network, 47K, 1/8W, 1206x2 Concave
R26	RES-47K5-0805-1T00	resistor, 47.5K, 0805, 1%
R32	RES-47K5-0805-1T00	resistor, 47.5K, 0805, 1%
R59	RES-4K70-0805-1T00	resistor, 4.7K, 0805, 1%
S1	SW__Panasonic_EVQ-PAE04M	pushbutton
U1	IC__ATMEL_ATmega644P-20PU	ATmega644P-20PU, 64K/4K/2K, 20MHz
U4	VREG__On-Semi_MC33269T-3.3G	voltage regulator, 3.3V, 800mA, TO-220
U10	FTDI_FT232RL	
U21	IC_DAC__TI_TLV5618	IC, DAC, TLV5618, 2ch, 12bit, DIP-8
U22	IC_REF__LM4041AIZ-1.2	IC, REF, 1.225V, 0.1%, TO-92

PRELIMINARY

Reference	Part Number	Description
U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1377+
U24	Molex_502702-0891	
U55	TI_SN65220DBV	
X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
	DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
	DIP-40P-600M	DIP Socket, 40 Pin, 600mil centers
	JMP__Adamtech_MSBHG	Shunt with handle
	BAT-CR1220	battery, coin cell, CR1220
	wiblock_NB2AS-PCB	

PRELIMINARY

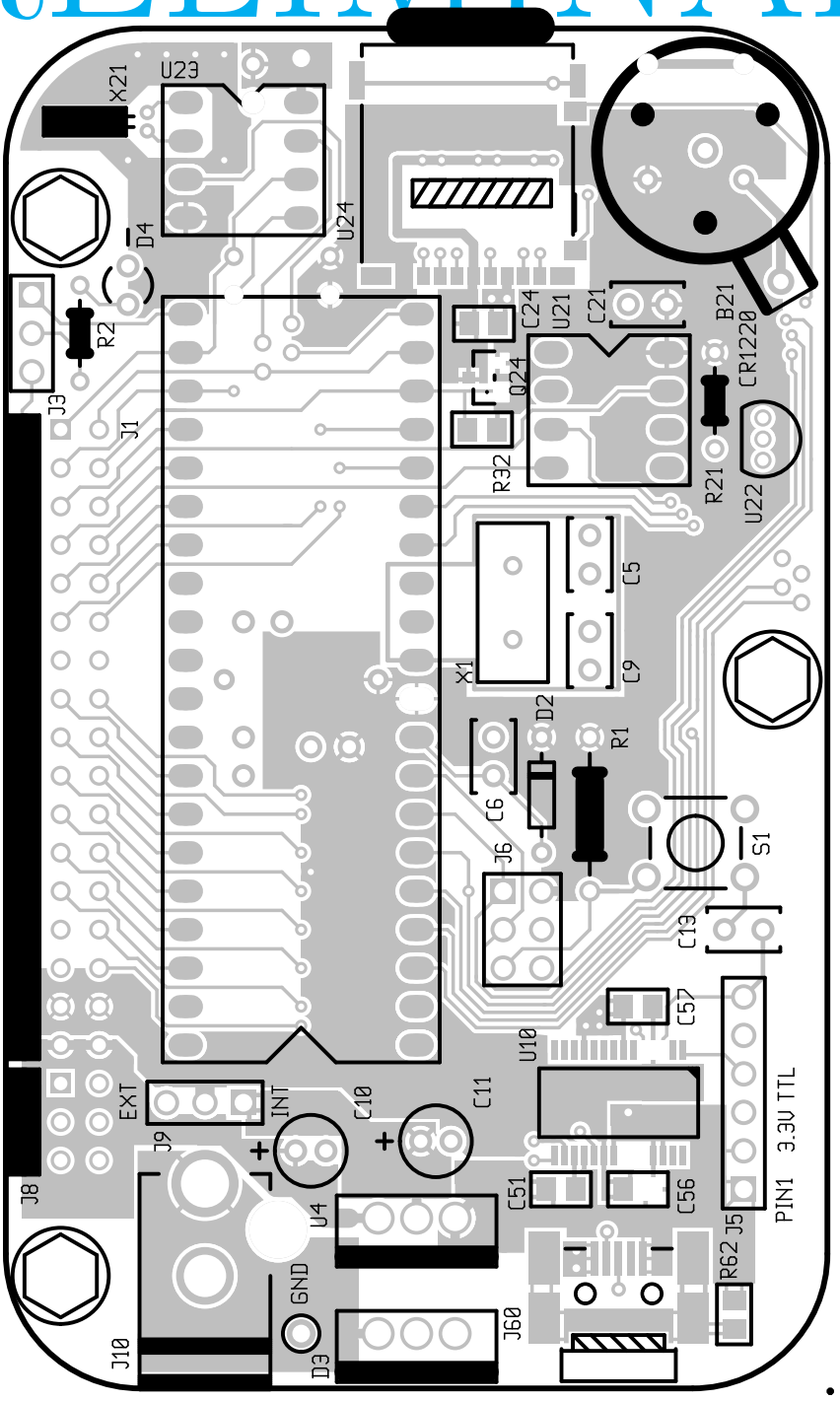


Figure 1: NB2AS Top Side Assembly Drawing (Rev 1)

PRELIMINARY

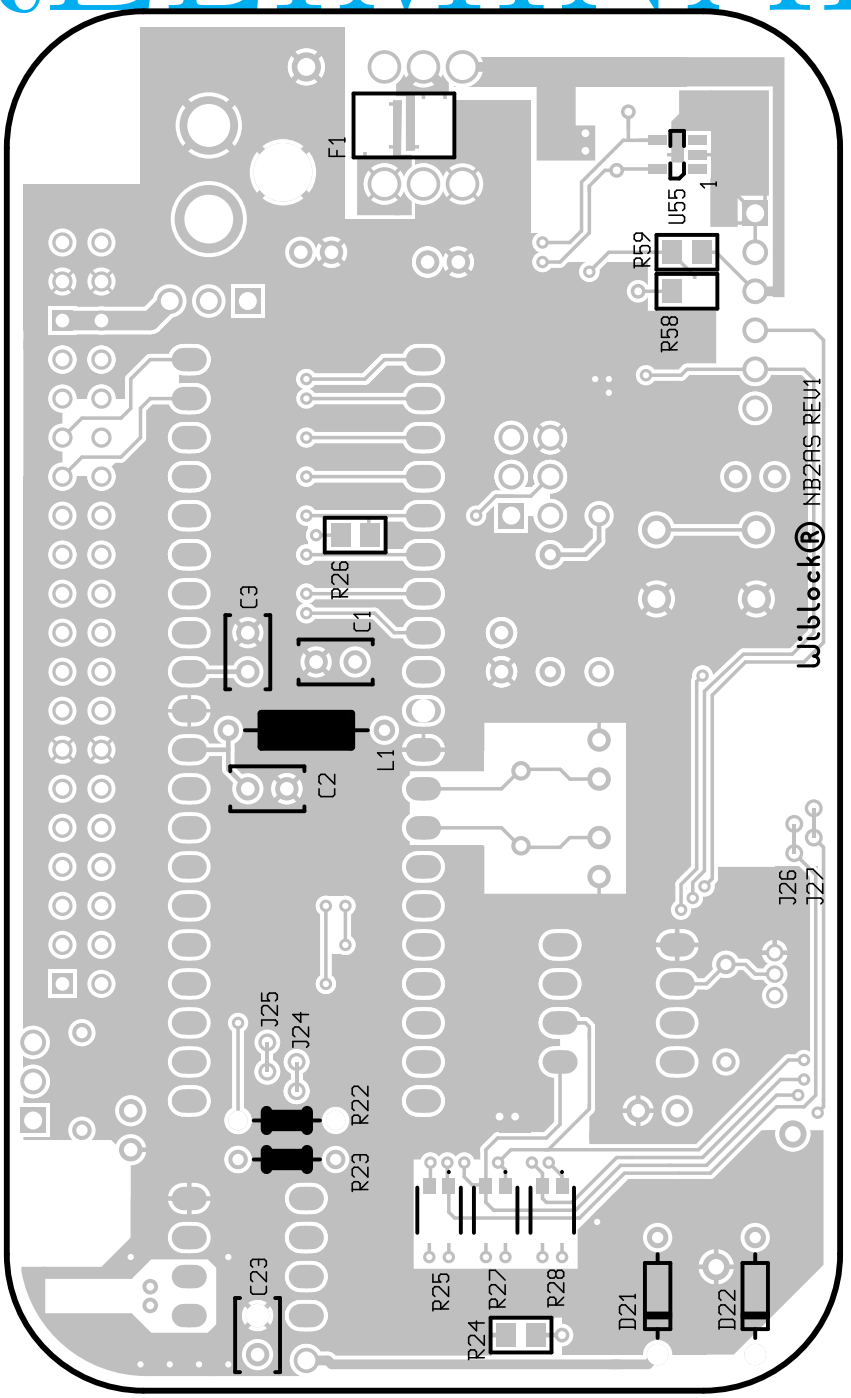


Figure 2: NB2AS Bottom Side Assembly Drawing (Rev 1)

PRELIMINARY

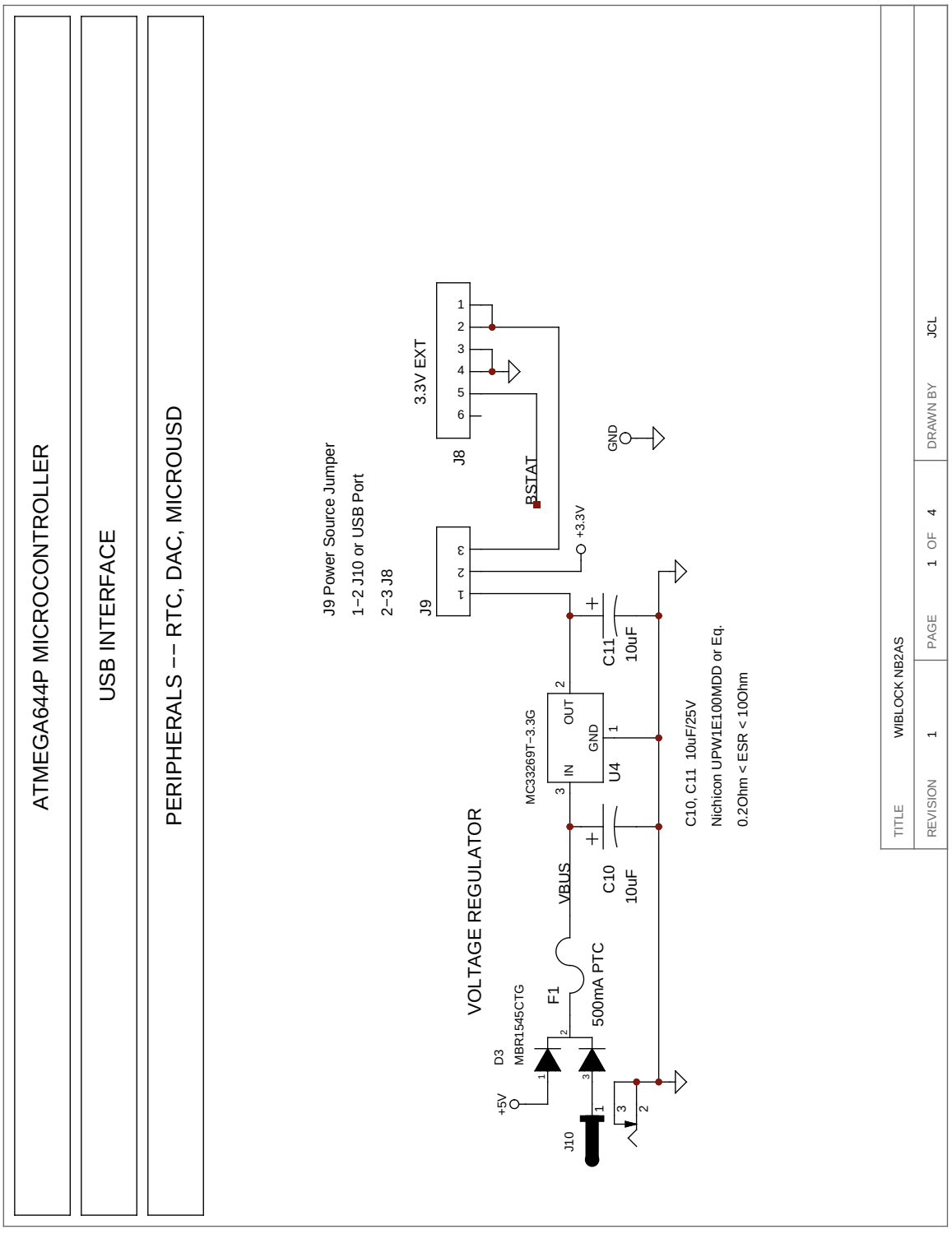


Figure 3: NB2AS (Rev 1)

PRELIMINARY

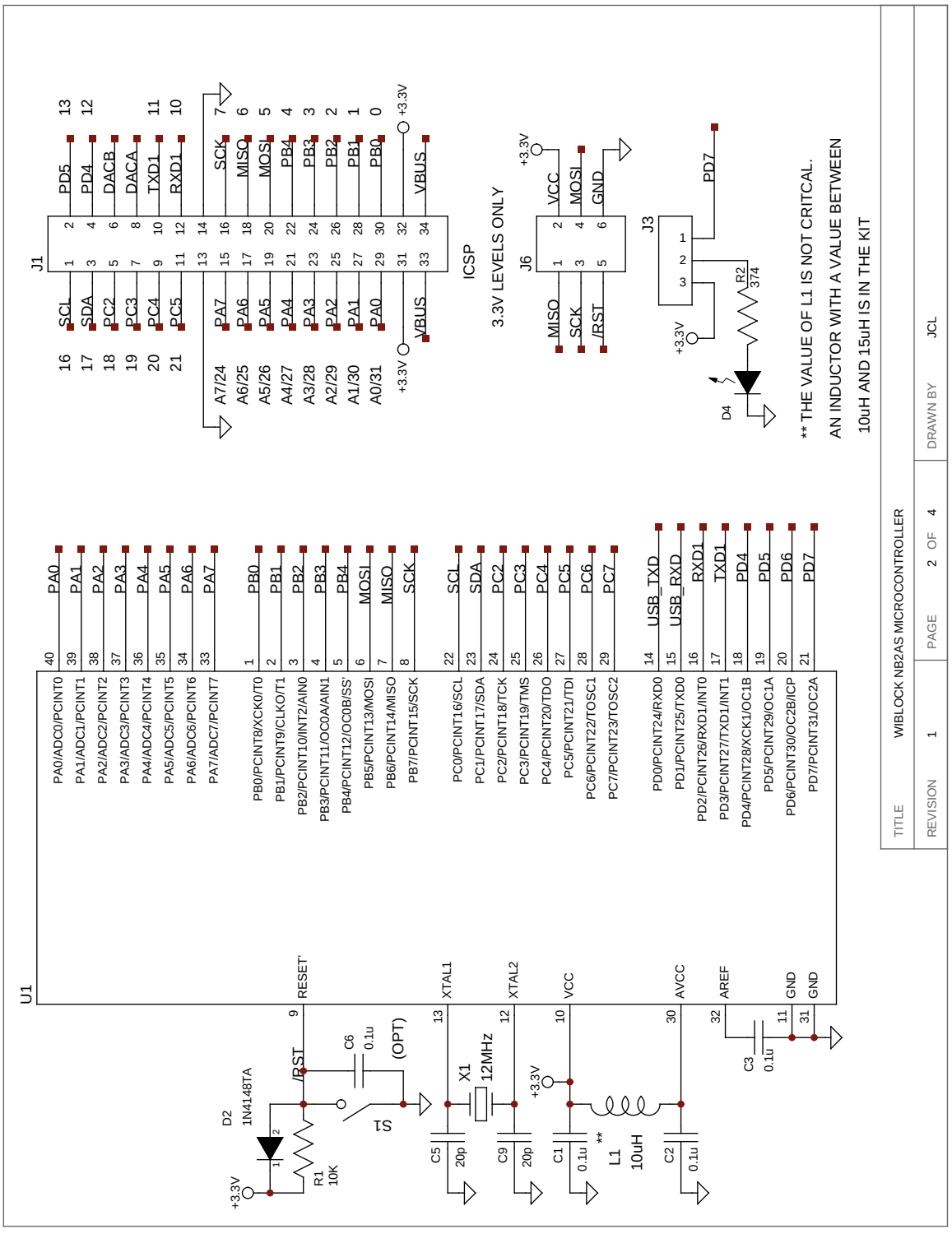


Figure 4: NB2AS (Rev 1)

PRELIMINARY

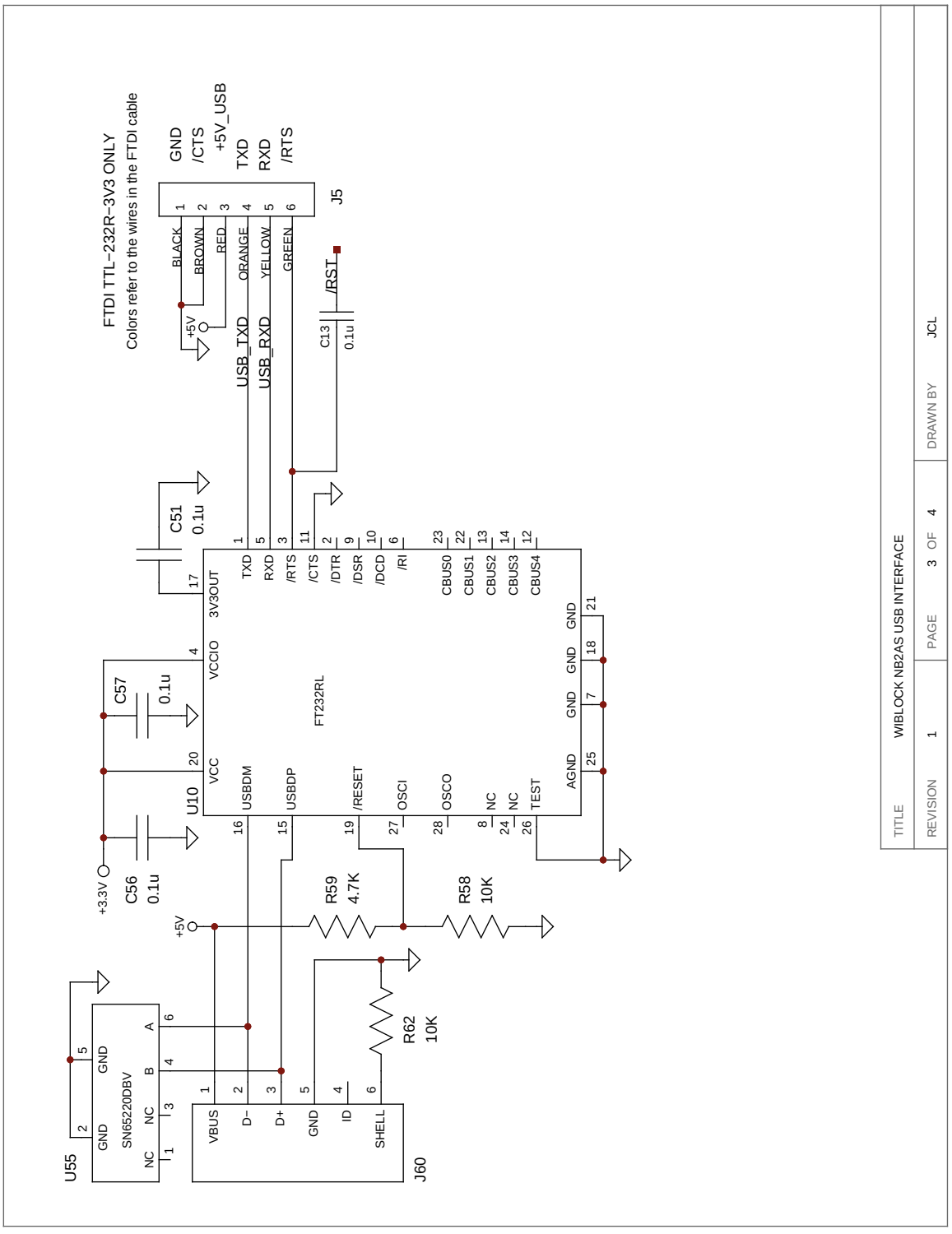


Figure 5: NB2AS (Rev 1)

PRELIMINARY

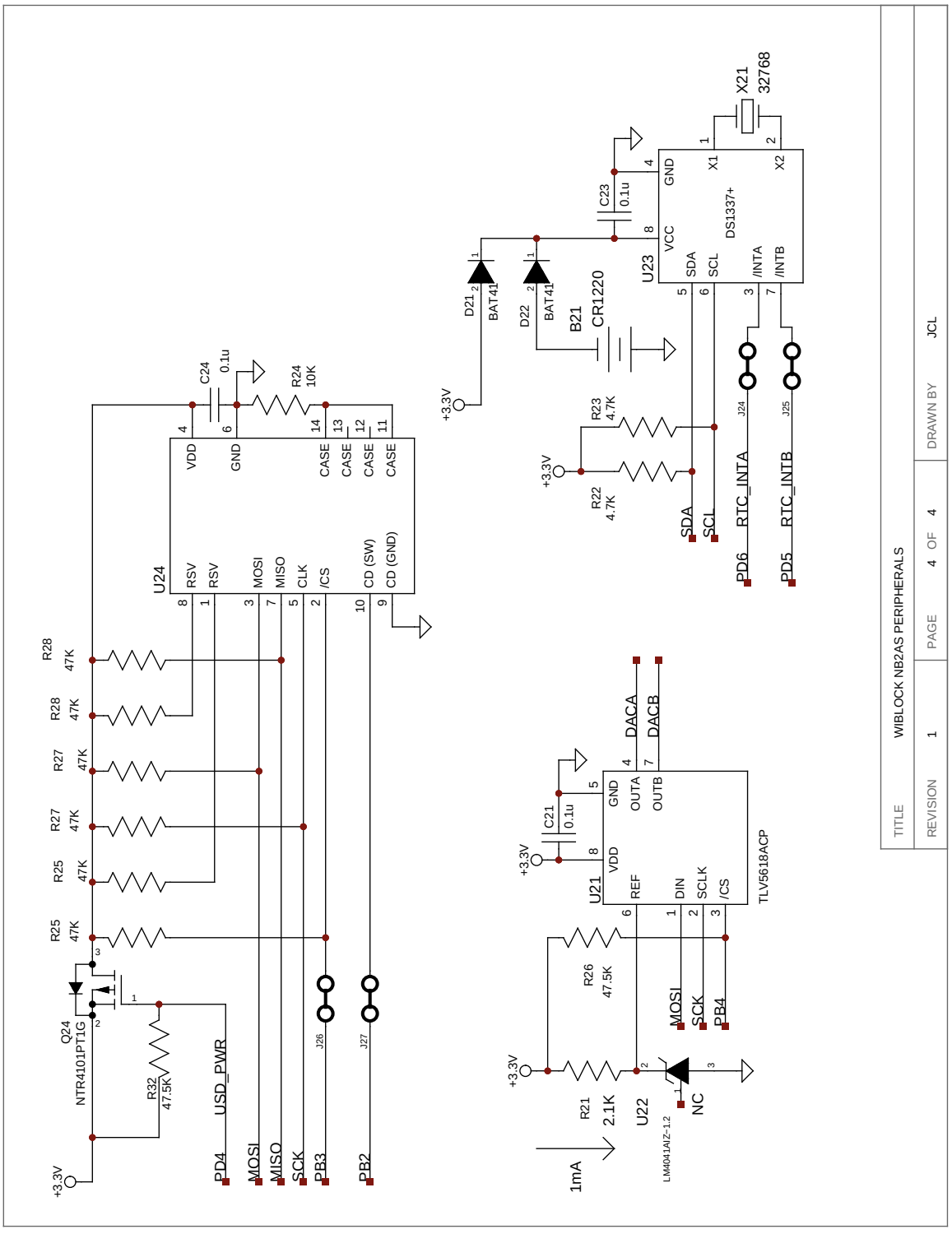


Figure 6: NB2AS (Rev 1)

PRELIMINARY

TLV5618A
2.7-V TO 5.5-V LOW-POWER DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

SLAS230H – JULY 1999 – REVISED JULY 2002

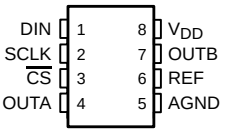
features

- Dual 12-Bit Voltage Output DAC
- Programmable Settling Time
  - 3 μs in Fast Mode
  - 10 μs in Slow Mode
- Compatible With TMS320 and SPI Serial Ports
- Differential Nonlinearity <0.5 LSB Typ
- Monotonic Over Temperature
- Direct Replacement for TLC5618A (C and I Suffixes)
- Available in Q-Temp Automotive
  HighRel Automotive Applications
  Configuration Control/Print Support
  Qualification to Automotive Standards

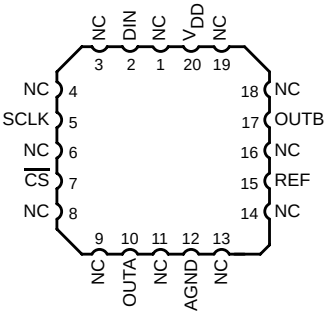
applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

P, D OR JG PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The TLV5618A is a dual 12-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface is compatible with TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

The resistor string output voltage is buffered by an x2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation.

Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package in standard commercial and industrial temperature ranges.

The TLV5618AC is characterized for operation from 0°C to 70°C. The TLV5618AI is characterized for operation from –40°C to 85°C. The TLV5618AQ is characterized for operation from –40°C to 125°C. The TLV5618AM is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	PLASTIC DIP (P)	SOIC (D)	CERAMIC DIP (JG)	20 PAD LCCC (FK)
0°C to 70°C	TLV5618ACP	TLV5618ACD	—	—
–40°C to 85°C	TLV5618AIP	TLV5618AID	—	—
–40°C to 125°C	—	TLV5618AQD TLV5618AQDR	—	—
–55°C to 125°C	—	—	TLV5618AMJG	TLV5618AMFK

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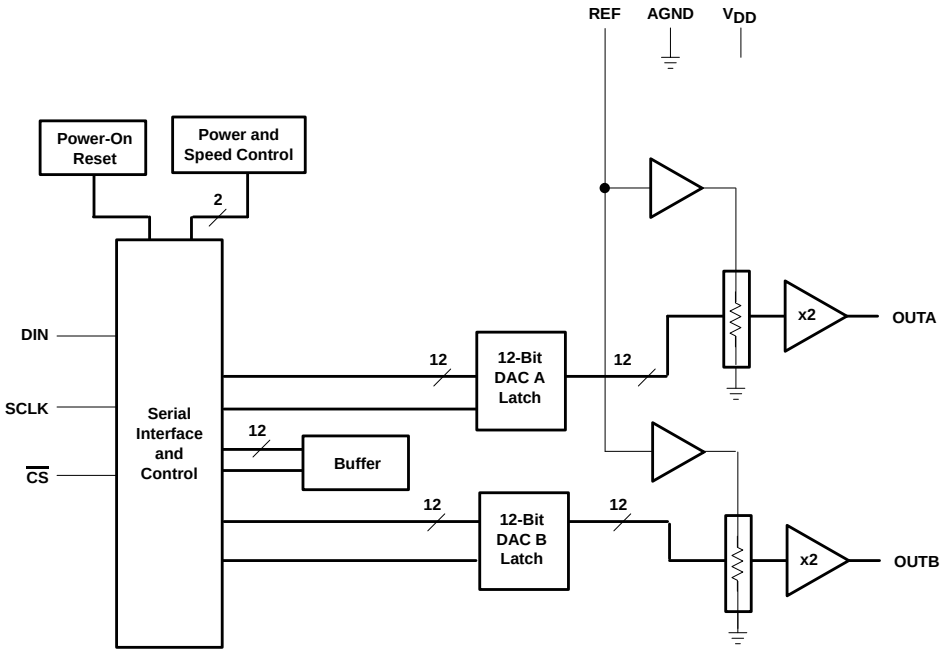
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRELIMINARY

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{CS}$	3	I	Chip select. Digital input active low, used to enable/disable inputs.
DIN	1	I	Digital serial data input
OUTA	4	O	DAC A analog voltage output
OUTB	7	O	DAC B analog voltage output
REF	6	I	Analog reference voltage input
SCLK	2	I	Digital serial clock input
V_{DD}	8	P	Positive power supply

TEXAS INSTRUMENTS
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PRELIMINARY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . . 7 V
Reference input voltage range . . . . . – 0.3 V to V_{DD} + 0.3 V
Digital input voltage range . . . . . – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5618AC . . . . . 0°C to 70°C
TLV5618AI . . . . . –40°C to 85°C
TLV5618AQ . . . . . –40°C to 125°C
TLV5618AM . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	635 mW	5.08 mW/°C	407 mW	330 mW	127 mW
FK	1375 mW	11.00 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.40 mW/°C	672 mW	546 mW	210 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R\Theta_{JA}$). Thermal resistances are not production tested and are for informational purposes only.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	
Power on reset		0.55		2	V
High-level digital input voltage, V_{IH}	V_{DD} = 2.7 V	2			V
	V_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	V_{DD} = 2.7 V			0.6	V
	V_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (see Note 1)	AGND	2.048	V_{DD}–1.5	V
	V_{DD} = 3 V (see Note 1)	AGND	1.024	V_{DD}–1.5	
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, $f_{(CLK)}$				20	MHz
Operating free-air temperature, T_A	TLV5618AC	0		70	°C
	TLV5618AI	–40		85	
	TLV5618AQ	–40		125	
	TLV5618AM	–55		125	

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ (V_{DD}–0.4 V)/2 causes clipping of the transfer function.

PRELIMINARY

electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = All ones	V_{DD} = 4.5 V to 5.5 V	C & I suffixes	Fast		1.8	2.5	mA
					Slow		0.8	1	
			V_{DD} = 2.7 V to 3.3 V		Fast		1.6	2.2	mA
					Slow		0.6	0.9	
			V_{DD} = 2.7 V to 5.5 V	M & Q suffixes	Fast		1.8	2.3	mA
					Slow		0.8	1	
	Power down supply current						1		µA
PSRR	Power supply rejection ratio		Zero scale, See Note 2				–65		dB
			Full scale, See Note 3				–65		

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_{ZS}(V_{DD}max) – E_{ZS}(V_{DD}min)/V_{DD}max]
3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_G(V_{DD}max) – E_G(V_{DD}min)/V_{DD}max]

static DAC specifications

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
	Resolution				12			bits
INL	Integral nonlinearity	See Note 4				±2	±4	LSB
DNL	Differential nonlinearity	See Note 5				±0.5	±1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See Note 6					±12	mV
E_{ZS} (TC)	Zero-scale-error temperature coefficient	See Note 7				3		ppm/°C
E_G	Gain error	See Note 8	C & I suffixes	V_{DD} = 4.5 V – 5.5 V			±0.29	% full scale V
				V_{DD} = 2.7 V – 3.3 V			±0.6	
			M & Q suffixes	V_{DD} = 2.7 V – 5.5 V			±0.6	
E_G (TC)	Gain-error temperature coefficient	See Note 9				1		ppm/°C

NOTES: 4. The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero-code and full-scale errors.
5. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/2V_{ref} × 10^6/(T_{max} – T_{min}).
8. Gain error is the deviation from the ideal output (2V_{ref} – 1 LSB) with an output load of 10 kΩ.
9. Gain temperature coefficient is given by: E_G T_C = [E_G (T_{max}) – E_g (T_{min})]/2V_{ref} × 10^6/(T_{max} – T_{min}).

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage range	R_L = 10 kΩ	0		V_{DD}–0.4	V
	Output load regulation accuracy	V_O = 4.096 V, 2.048 V, R_L = 2 kΩ to 10 kΩ			±0.29	% FS

PRELIMINARY

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

reference input

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		$V_{DD}-1.5$	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc	Fast		1.3		MHz
			Slow		525		kHz
	Reference feedthrough	REF = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 10)			–80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V	–1			µA
C_i	Input capacitance			8		pF

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, See Note 11	Fast		1	3	µs
			Slow		3	10	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, See Note 12	Fast		1		µs
			Slow		2		
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See Note 13	Fast		3		V/µs
			Slow		0.5		
	Glitch energy	DIN = 0 to 1, FCLK = 100 kHz, $\overline{CS}$ = V_{DD}			5		nV–s
SNR	Signal-to-noise ratio	f_S = 102 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF			76		dB
SINAD	Signal-to-noise + distortion				68		
THD	Total harmonic distortion				–68		
SFDR	Spurious free dynamic range				72		

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full-scale voltage.

PRELIMINARY

digital input timing requirements

				MIN	NOM	MAX	UNIT
$t_{su(CS-CK)}$	Setup time, $\overline{CS}$ low before first negative SCLK edge	C and I suffixes	V_{DD} = 5 V	5			ns
			V_{DD} = 3 V	10			
		Q and M suffixes		10			ns
$t_{su(C16-CS)}$	Setup time, 16th negative SCLK edge before $\overline{CS}$ rising edge			10			ns
$t_{w(H)}$	SCLK pulse width high			25			ns
$t_{w(L)}$	SCLK pulse width low			25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	C and I suffixes	V_{DD} = 5 V	5			ns
			V_{DD} = 3 V	10			
		Q and M suffixes		8			
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	C and I suffixes	V_{DD} = 5 V	5			ns
			V_{DD} = 3 V	10			
		Q and M suffixes		10			
$t_{h(CSH)}$	Hold time, $\overline{CS}$ high between cycles		V_{DD} = 5 V	25			ns
			V_{DD} = 3 V	50			

timing requirements

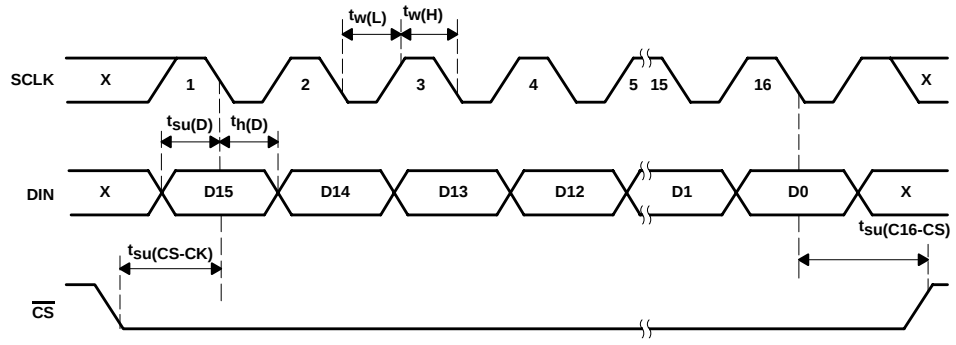

Figure 1. Timing Diagram

PRELIMINARY

TYPICAL CHARACTERISTICS

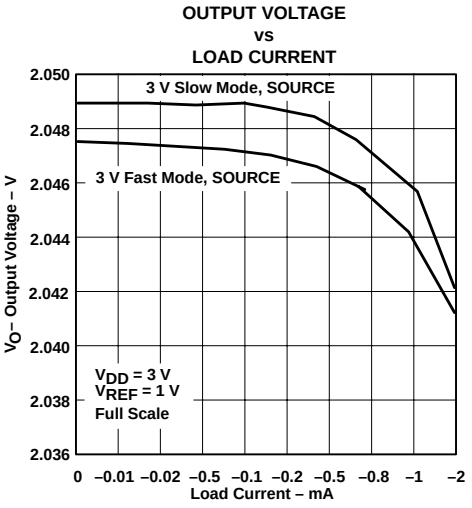

Figure 2

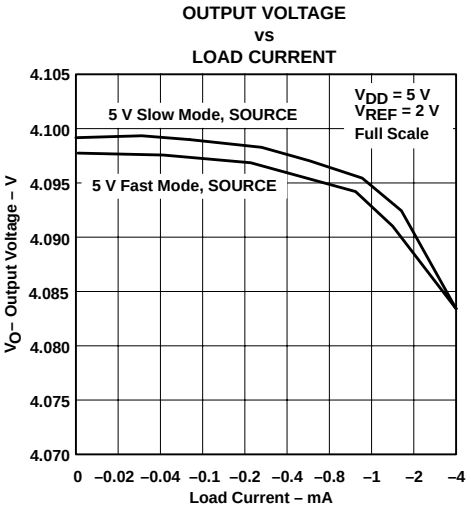

Figure 3

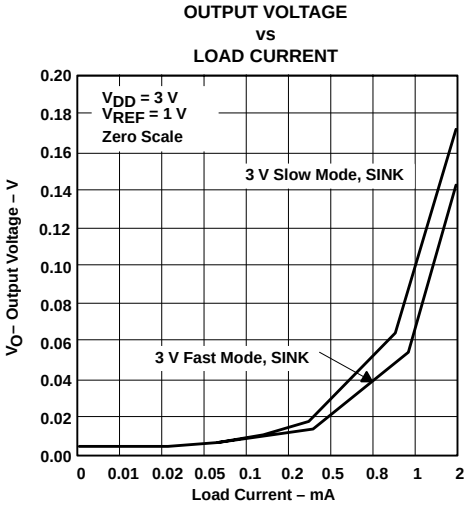

Figure 4

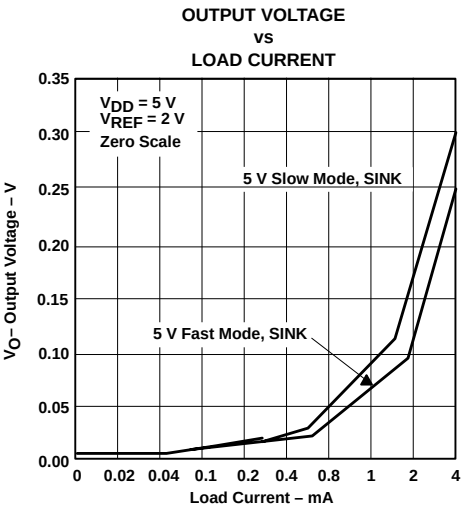

Figure 5

PRELIMINARY

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

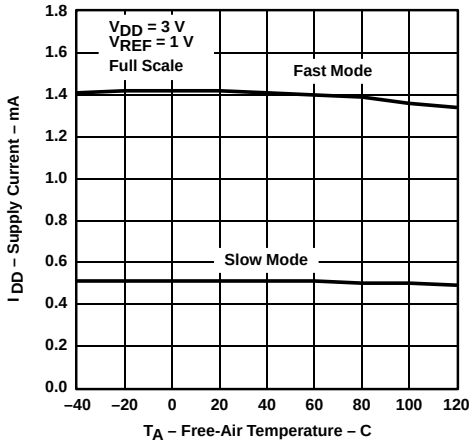

Figure 6

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

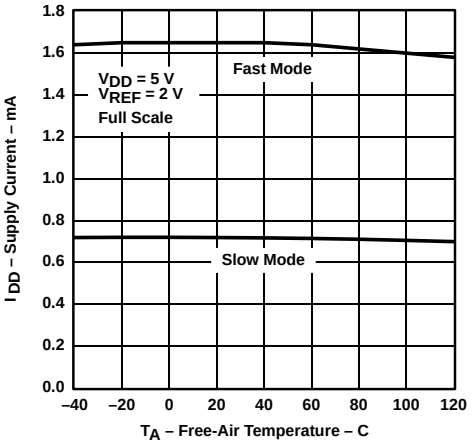

Figure 7

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

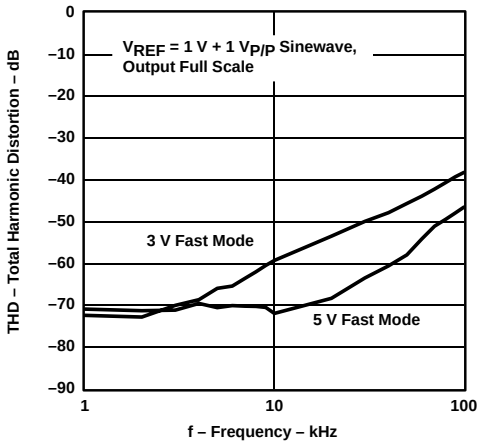

Figure 8

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

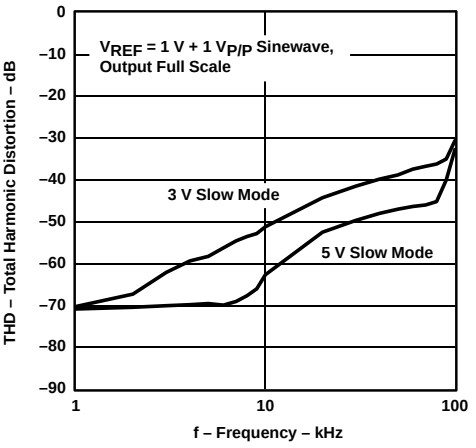

Figure 9

TEXAS INSTRUMENTS
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PRELIMINARY

TYPICAL CHARACTERISTICS

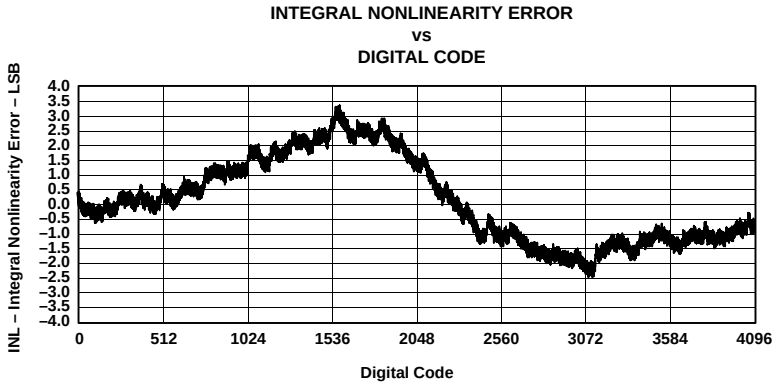

Figure 10

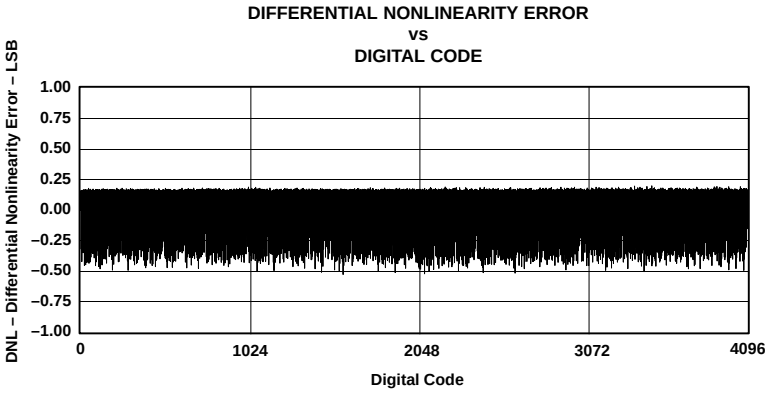

Figure 11

PRELIMINARY

APPLICATION INFORMATION

general function

The TLV5618A is a dual 12-bit, single-supply DAC, based on a resistor-string architecture. It consists of a serial interface, a speed and power down control logic, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by the reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{2^n}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to 2^n–1, where n=12 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

A falling edge of $\overline{CS}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{CS}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 12 shows examples of how to connect the TLV5618A to TMS320, SPI, and Microwire.

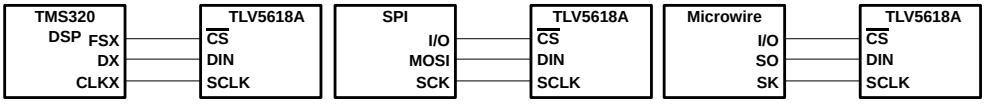

Figure 12. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to $\overline{CS}$. If the word width is 8 bits (SPI and Microwire) two write operations must be performed to program the TLV5618A. After the write operation(s), the holding registers or the control register are updated automatically on the next positive clock edge following the 16^{th} falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20\ \mathrm{MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.25\ \mathrm{MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5618A should also be considered.

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APPLICATION INFORMATION

data format

The 16-bit data word for the TLV5618A consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	MSB											LSB
				12 Data bits											

SPD: Speed control bit 1 → fast mode 0 → slow mode
PWR: Power control bit 1 → power down 0 → normal operation
On power up, SPD and PWD are reset to 0 (slow mode and normal operation)

The following table lists all possible combinations of register-select bits:

register-select bits

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Reserved

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

examples of operation

- Set DAC A output, select fast mode:

  Write new DAC A value and update DAC A output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A output value											

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC B output, select fast mode:

  Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New BUFFER content and DAC B output value											

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC A value, set DAC B value, update both simultaneously, select slow mode:

  1. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value											

  2. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value											

PRELIMINARY

APPLICATION INFORMATION

examples of operation (continued)

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

- Set power-down mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Don't care

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 13.

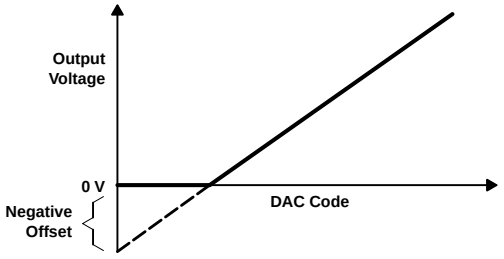

Figure 13. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

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APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

total harmonic distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

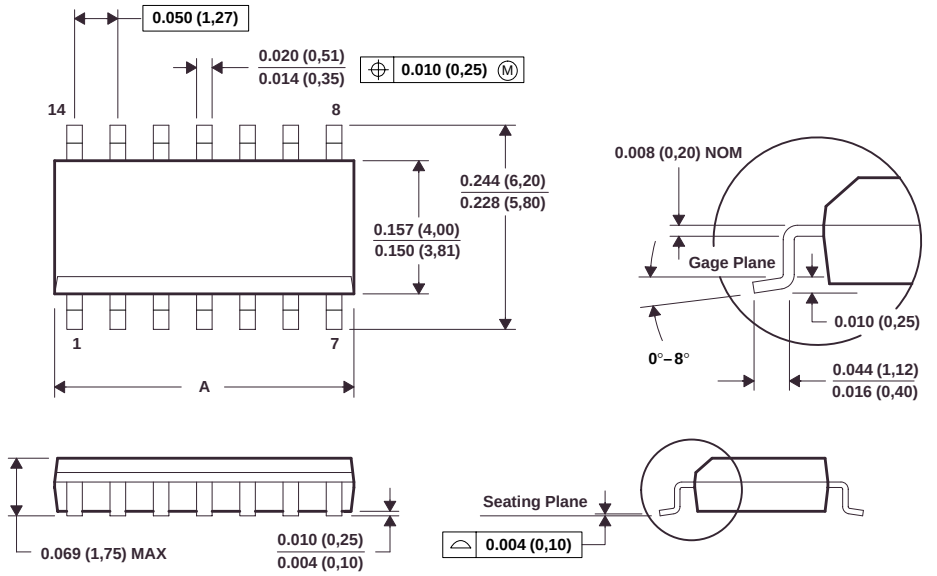
Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

PRELIMINARY

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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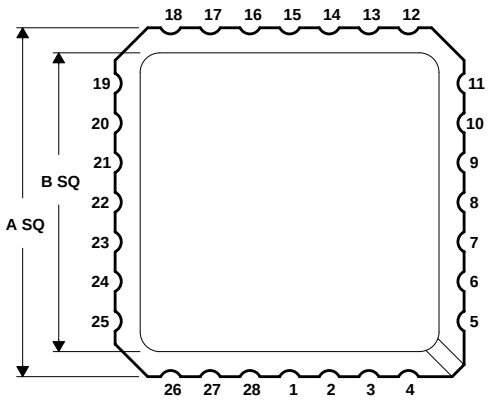
PRELIMINARY

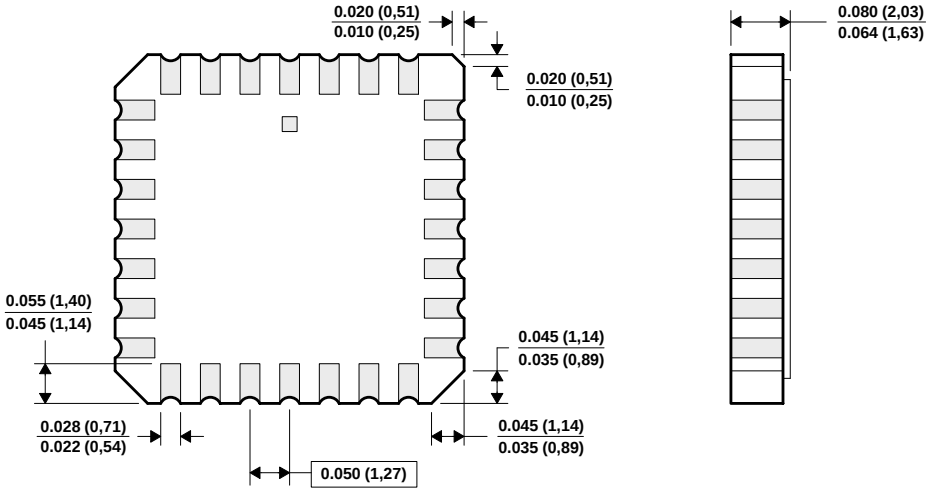
MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINALS SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



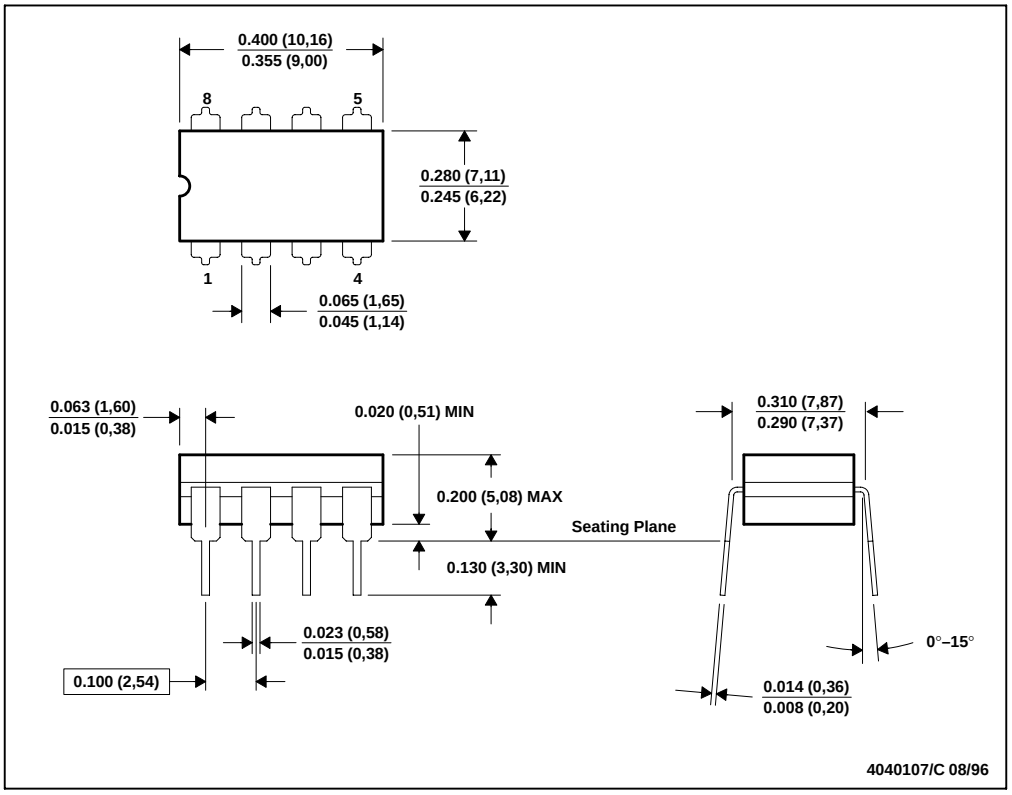
4040140 / C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold-plated.
E. Falls within JEDEC MS-004

PRELIMINARY

MECHANICAL DATA

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

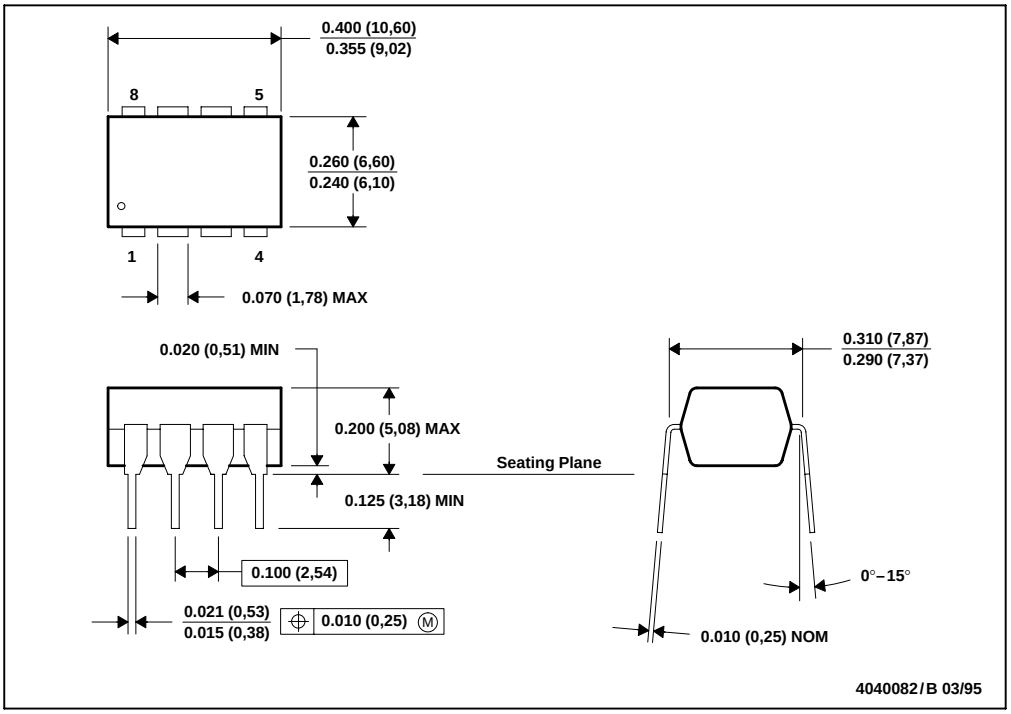


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

PRELIMINARY

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PRELIMINARY

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PRELIMINARY

19-4652; 7/09

DALLAS SEMICONDUCTOR MAXIM

DS1337
I²C Serial Real-Time Clock

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V. I^2C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with V_{CC} as low as 1.3V.

APPLICATIONS

Handhelds (GPS, POS Terminal, MP3 Player)

Consumer Electronics (Set-Top Box, VCR/Digital Recording)

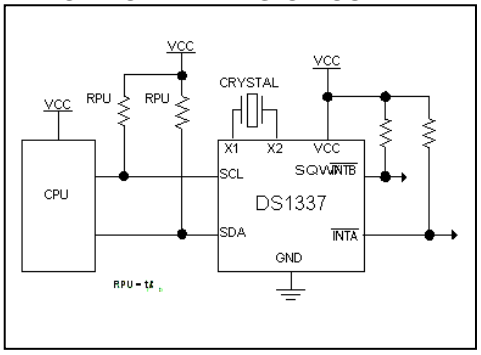
Office Equipment (Fax/Printer, Copier)

Medical (Glucometer, Medicine Dispenser)

Telecommunications (Router, Switch, Server)

Other (Utility Meter, Vending Machine, Thermostat, Modem)

TYPICAL OPERATING CIRCUIT



FEATURES

- **Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100**
- **Available in a Surface-Mount Package with an Integrated Crystal (DS1337C)**
- **I^2C Serial Interface**
- **Two Time-of-Day Alarms**
- **Oscillator Stop Flag**
- **Programmable Square-Wave Output Defaults to 32kHz on Power-Up**
- **Available in 8-Pin DIP, SO, or µSOP**
- **-40°C to +85°C Operating Temperature Range**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1337+	-40°C to +85°C	8 DIP (300 mils)	DS1337
DS1337S+	-40°C to +85°C	8 SO (150 mils)	DS1337
DS1337U+	-40°C to +85°C	8 µSOP	1337
DS1337C#	-40°C to +85°C	16 SO (300 mils)	DS1337C

+ Denotes a lead(Pb)-free/RoHS-compliant device.
 # Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.
† A "+" anywhere on the top mark denotes a lead-free device. A "#" denotes a RoHS-compliant device.

Pin Configurations appear at end of data sheet.

***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.*

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.3V to +6.0V
Operating Temperature Range (Noncondensing).....-40°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	Full operation	1.8	3.3	5.5	V
	V_{CCT}	Timekeeping (Note 5)	1.3		1.8	V
Logic 1	V_{IH}	SCL, SDA	0.7 x V_{CC}		V_{CC} + 0.3	V
		$\overline{INTA}$, SQW/$\overline{INTB}$			5.5	
Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS—Full Operation

(**V_{CC} = 1.8V to 5.5V**, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 2)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 3)	-1		+1	µA
Logic 0 Output (V_{OL} = 0.4V)	I_{OL}	(Note 3)			3	mA
Active Supply Current	I_{CCA}	(Note 4)			150	µA
Standby Current	I_{CCS}	(Notes 5, 6)			1.5	µA

DC ELECTRICAL CHARACTERISTICS--Timekeeping

(**V_{CC} = 1.3V to 1.8V,** T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timekeeping Current (Oscillator Enabled)	I_{CCTOSC}	(Notes 5, 7, 8, 9)		425	600	nA
Data-Retention Current (Oscillator Disabled)	I_{CCTDDR}	(Notes 5, 9)			100	nA

PRELIMINARY

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 14)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 15)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}			100		ms

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{INTA}$, and SQW/$\overline{INTB}$.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 5: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when $1.8 \le V_{CC} \le 5.5V$. Time and date are maintained when $1.3V \le V_{CC} \le 1.8V$.

Note 10: After this period, the first clock pulse is generated

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \ge$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Note 14: C_B—total capacitance of one bus line in pF.

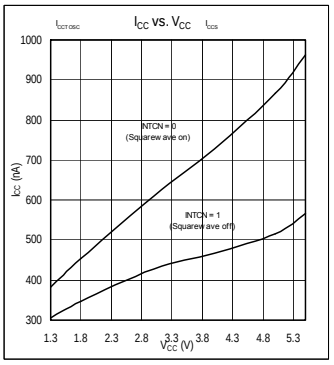
Note 15: Guaranteed by design. Not production tested.

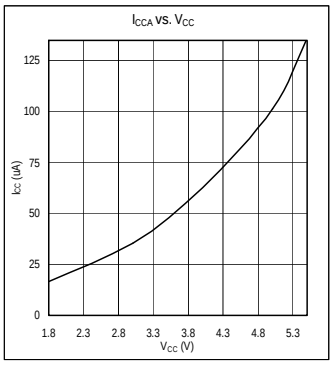
PRELIMINARY

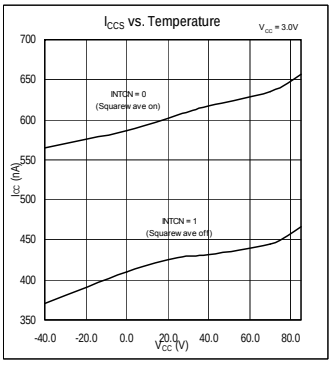
Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF bit to be set over the voltage range of $V_{CC(MIN)} \le V_{CC} \le V_{CC(MAX)}$..

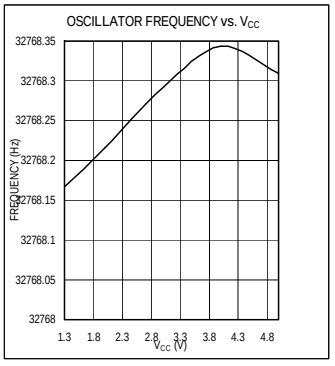
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)







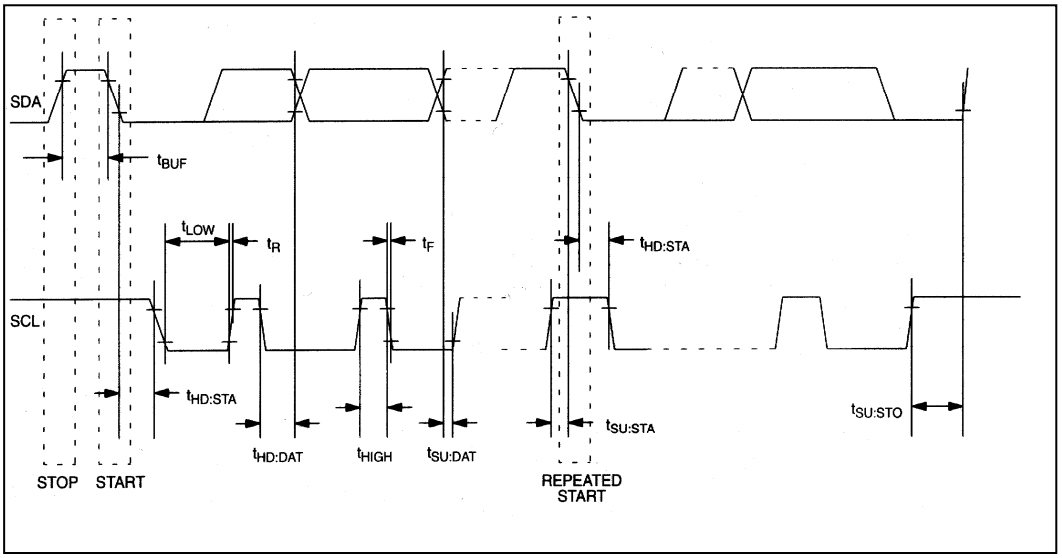


PRELIMINARY

PIN DESCRIPTION

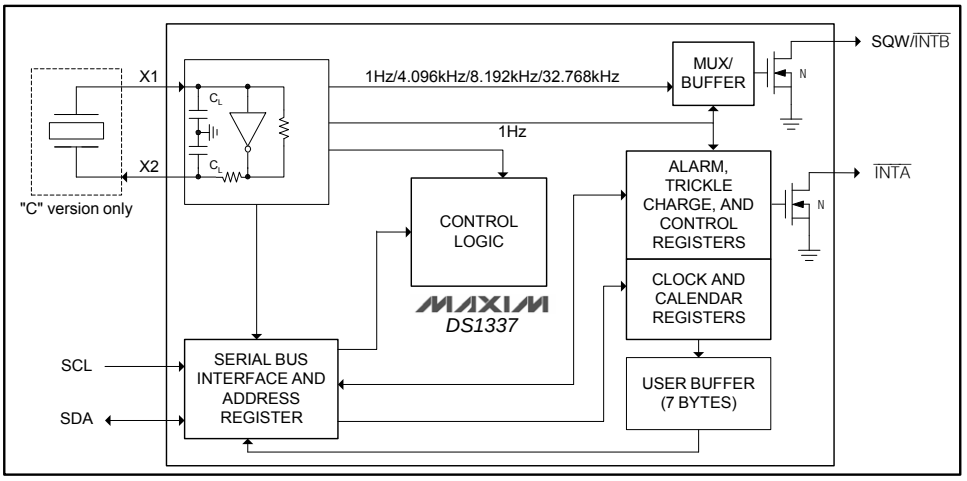
PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. An external 32.768kHz oscillator can also drive the DS1337. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	—	X2	
3	14	$\overline{INTA}$	Interrupt Output. When enabled, $\overline{INTA}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
4	15	GND	Ground. DC power is provided to the device on this pin.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain output and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the serial interface.
7	2	SQW/$\overline{INTB}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
8	3	V_{CC}	DC Power. DC power is provided to the device on this pin.
—	4–13	N.C.	No Connect. These pins are not connected internally, but must be grounded for proper operation.

TIMING DIAGRAM



PRELIMINARY

BLOCK DIAGRAM



DETAILED DESCRIPTION

The *Block Diagram* shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over an I²C bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever V_{CC} is between 5.5V and 1.8V. I²C operation is not guaranteed when V_{CC} is below 1.8V. The DS1337 maintains the time and date when V_{CC} is as low as 1.3V.

OSCILLATOR CIRCUIT

The DS1337 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

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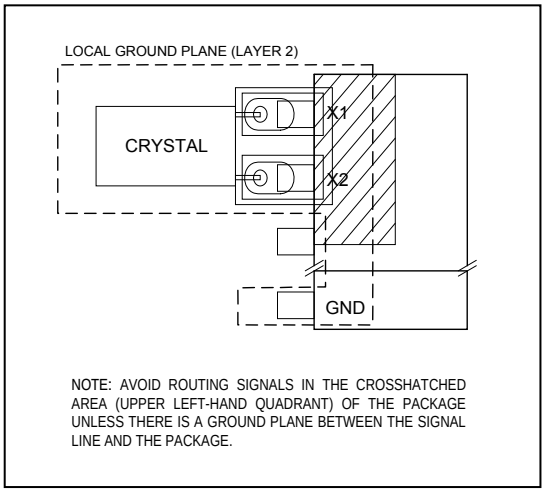
CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Figure 1. Typical PC Board Layout for Crystal



DS1337C ONLY

The DS1337C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately +10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

OPERATING MODES

The amount of current consumed by the DS1337 is determined, in part, by the I²C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V_{CC}	Power
I²C Interface Active	1.8V ≤ V_{CC} ≤ 5.5V	I_{CC} Active (I_{CCA})
I²C Interface Inactive	1.8V ≤ V_{CC} ≤ 5.5V	I_{CC} Standby (I_{CCS})
I²C Interface Inactive	1.3V ≤ V_{CC} ≤ 1.8V	Timekeeping (I_{CCTOSC})
I²C Interface Inactive Oscillator Disabled	1.3V ≤ V_{CC} ≤ 1.8V	Data Retention (I_{CCTDDR})

PRELIMINARY

ADDRESS MAP

Table 2 shows the address map for the DS1337 registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Minutes			Minutes				Minutes	00–59
02H	0	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Hours	1–12 +AM/PM 00–23
03H	0	0	0	0	0	Day			Day	1–7
04H	0	0	10 Date		Date				Date	01–31
05H	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06H	10 Year				Year				Year	00–99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09H	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0AH	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	01–31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0CH	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
0DH	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	01–31
0EH	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied or V_{CC} falls below the V_{OSC}.*

I²C INTERFACE

The I²C interface is accessible whenever V_{CC} is at a valid level. If a microcontroller connected to the DS1337 resets while reading from the DS1337 during an I²C read, the two could become unsynchronized. The microcontroller must terminate the last byte read with a Not-Acknowledge (NACK) to properly terminate the read. When the microcontroller resets, the DS1337 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

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CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 2. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{\text{AM}}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/$\overline{24}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 3 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{\text{DT}}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/$\overline{\text{DT}}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{\text{DT}}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. The bit(s) will remain at a logic 1 until written to a logic 0 by the user. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$) signals. The match is tested on the once-per-second update of the time and date registers.

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Table 3. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQW/$\overline{INTB}$ Output

INTCN	RS2	RS1	SQW/$\overline{INTB}$ OUTPUT	A2IE
0	0	0	1Hz	X
0	0	1	4.096kHz	X
0	1	0	8.192kHz	X
0	1	1	32.768kHz	X
1	X	X	$\overline{A2F}$	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers l activates the $\overline{INTA}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{INTB}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INTB}$ pin. This bit is set to logic 0 when power is first applied.

PRELIMINARY

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INTA}$ (when INTCN = 0) or to assert SQW/$\overline{INTB}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INTA}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{INTA}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} is insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{INTA}$ or SQW/$\overline{INTB}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{INTA}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{INTB}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{INTA}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

PRELIMINARY

I²C SERIAL DATA BUS

The DS1337 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1337 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1337 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

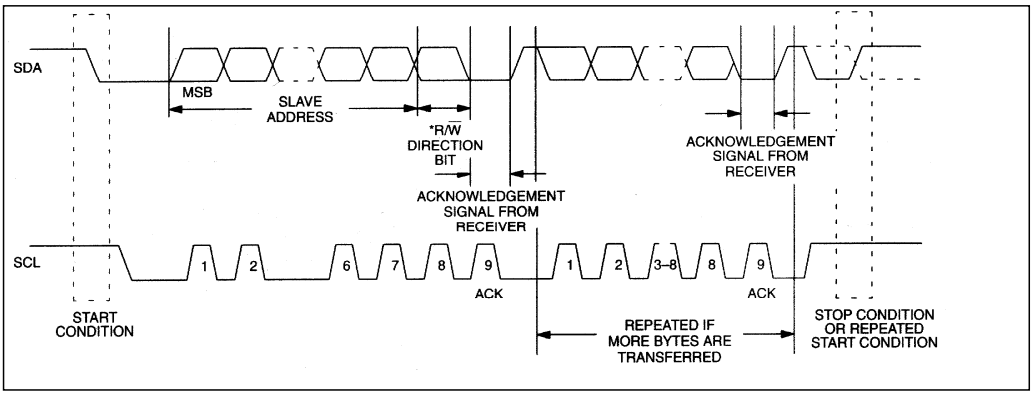
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

PRELIMINARY

Figure 2. Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1337 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 3). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This sets the register pointer on the DS1337. The master may then transmit zero or more bytes of data, with the DS1337 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 4 and Figure 5). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a “not acknowledge” to end a read.

PRELIMINARY

Figure 3. Data Write—Slave Receiver Mode

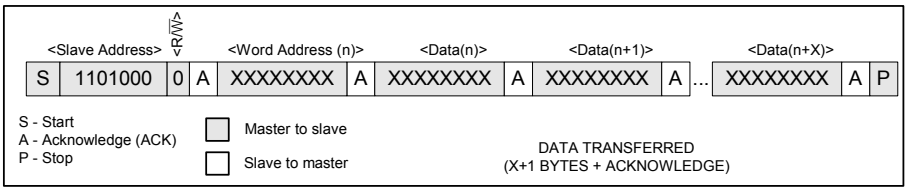


Figure 4. Data Read (from Current Pointer Location)—Slave Transmitter Mode

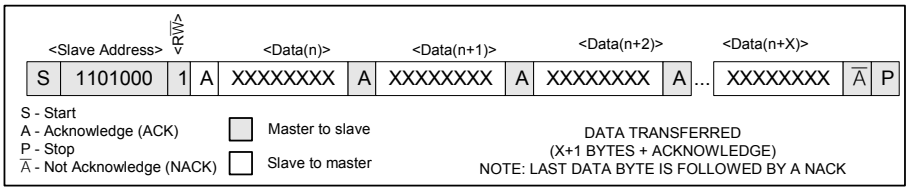
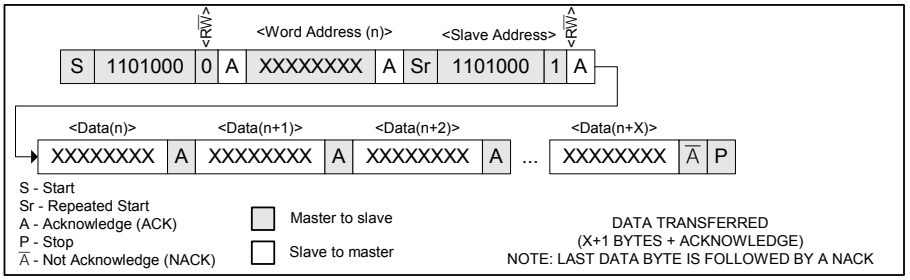


Figure 5. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



PRELIMINARY

HANDLING, PC BOARD LAYOUT, AND ASSEMBLY

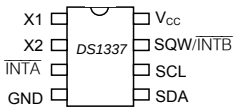
The DS1337C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

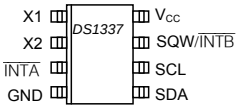
Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

PIN CONFIGURATIONS

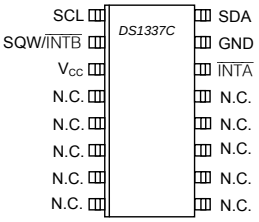
TOP VIEW



DIP



SO, µSOP



SO (300 mils)

CHIP INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL INFORMATION

PACKAGE	THETA-J_A (°C/W)	THETA-J_C (°C/W)
8 DIP	110	40
8 SO	170	40
8 µSOP	229	39
16 SO	73	23

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8+8	**21-0043**
8 SO	S8+2	**21-0041**
8 µMAX	U8+1	**21-0036**
16 SO	W16-H2	**21-0042**

PRELIMINARY

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
080508	Added device access details to *General Description* section.	1
	Removed leaded ordering numbers from the *Ordering Information* table.	1
	Added Note 5 to Timekeeping V_{CC} EC table range.	2
	Added “Full Operation” and “Timekeeping” to headers to clarify table usage.	2
	Added OSF parameter to EC table.	3
	Updated *Pin Description* to indicate max input voltage and that unused outputs may be left open.	5
	Added oscillator circuit and show open-drain transistors on *Block Diagram*.	6
	Added *Operating Mode* section with details on operating mode and corresponding Icc parameter.	7
	Added *I²C Interface* section explaining how to synchronize a microcontroller and the RTC.	8
	Corrected legend in figure 5 for not-acknowledge (add overbar to symbol).	14
071609	Removed conflicting SDA/SCL input bias statement in *Pin Description*.	5

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